Sebastian Liebig

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Bibliographic description

Optimization of rectifiers for aviation regarding power density and reliability

Sebastian Liebig

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rectifier, APFC, ATRU, active power filter, power quality, harmonics, EMC, SiC-MOSFET, reliability, cosmic radiation, lifetime, control, instantaneous power theory, selective signal analysis, phase locked loop

Abstract
The intentions of the so-called "More Electric Aircraft" (MEA) are higher efficiency and lower weight. A main topic here is the application of electrical instead of hydraulic, pneumatical and mechanical systems. The necessary power electronic devices have intermediate DC-links, which are typically supplied by a three-phase system with active B6 or passive B12 rectifiers. A possible alternative is the B6 diode bridge in combination with an active power filter (APF). Due to the parallel arrangement, the APF offers a higher power density and is able to compensate for harmonics from several devices. The use of the diode bridge rectifier alone is not permitted due to the highly distorted phase current.
The following investigations are dealing with the development of an active power filter for a three-phase supply with variable frequency from 360 to 800 Hz. All relevant components such as inductors, EMC-filters, power modules and DC-link capacitor are designed. A particular focus is put on the customized power module with SiC-MOSFETs and SiC-diodes, which is characterized electrically and thermally. The maximum supply frequency slope has a value of 50 Hz/ms, which requires a high dynamic and robustness on the control algorithm. Furthermore, the content of 5^{th} and 7^{th} harmonics must be reduced to less than 2 %, which demands a high accuracy. To cope with both requirements, a two-stage filter algorithm is developed and implemented in two independent signal processors. Simulations and laboratory experiments confirm the performance and robustness of the control algorithm.
This work comprehensively presents the design of aerospace rectifiers. The results were published in conferences and patents.

Bibliografische Beschreibung

Optimierung von Gleichrichtern für die Luftfahrt unter Berücksichtigung von Leistungsdichte und Zuverlässigkeit.

Sebastian Liebig

183 Seiten, 182 Abbildungen, 24 Tabellen

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Schlagwörter
Gleichrichter, aktiver Leistungsfilter, Netzrückwirkungen, EMV, Zuverlässigkeit, Lebensdauer, Höhenstrahlung, Regelung, selektive Signalanalyse

Kurzfassung
Hauptziele des sogenannten "More Electric Aircraft" (MEA) sind Effizienzerhöhung und Gewichtseinsparung. Ein Schwerpunkt hierbei ist die Nutzung von elektrischen statt hydraulischen, pneumatischen und mechanischen Systemen. Die notwendigen Leistungselektroniken haben DC-Zwischenkreise, welche mittels aktiven B6 oder passiven B12 Gleichrichtern aus dem Dreiphasennetz gespeist werden. Eine mögliche Alternative ist die B6 Diodenbrücke in Kombination mit einem aktiven Netzfilter, welcher aufgrund der parallelen Anordnung eine höhere Leistungsdichte aufweist und darüber hinaus mehrere Geräte gleichzeitig entstören kann. Die alleinige Nutzung einer Diodenbrücke ist aufgrund des hohen Anteils von Stromharmonischen nicht zulässig.
Diese Arbeit beschäftigt sich mit der Entwicklung eines aktiven Filters für ein Dreiphasensystem mit variabler Frequenz von 360 bis 800 Hz. Es werden alle relevanten Bauteile wie Induktivitäten, EMV-Filter, Leistungsmodule und Zwischenkreiskondensator ausgelegt. Besonderes Augenmerk liegt auf dem kundenspezifischen Modul mit SiC-Dioden und SiC-MOSFETs, welches vollständig elektrisch und thermisch charakterisiert wird. Die Änderung der Netzfrequenz beträgt bis zu 50 Hz/ms, was eine hohe Dynamik und Robustheit von der Filterregelung verlangt. Weiterhin ist im statischen Fall eine hohe Genauigkeit gefordert, da die 5. und 7. Harmonische auf unter 2% geregelt werden müssen. Um beiden Anforderungen gerecht zu werden, wird ein zweistufiger Regelungsalgorithmus entwickelt der auf zwei digitalen Signalprozessoren implementiert wird. Simulationen und Labormessungen bestätigen die Robustheit des Regelungskonzeptes.
Diese Arbeit stellt umfassend die Entwicklung von Luftfahrtgleichrichtern dar. Die Ergebnisse wurden in Konferenzen und Patenten veröffentlicht.

Contents

Inhaltsverzeichnis

Nomenclature

A_c	cross section of magnetic core	m^2
A_{comp}	amplitude of compensation current in frequency domain	A
A_C	Clarke transformation matrix	
A_{cc}	amplitude of G_{cc}	
A_{CE}	allowed limit for conducted emissions	A
A_{dc}	amplitude of DC-link voltage ripple in frequency domain	V
A_f	total area of floating parts of the APF	m^2
A_L	inductive constant	$H\ n^{-2}$
A_P	Parke transformation matrix	
A_{RE}	allowed limit for radiated emissions	$V\ m^{-1}$
B_{sat}	saturation flux in magnetic core	T
$\hat{B}$	peak flux in magnetic core	T
C_d	capacitance in LCR damping circuit	F
C_{D1}	first thermal capacitor of foster model of a diode	$J\ K^{-1}$
C_{D2}	second thermal capacitor of foster model of a diode	$J\ K^{-1}$
C_{D3}	third thermal capacitor of foster model of a diode	$J\ K^{-1}$
C_{dc}	DC-link capacitance of load DC-link	F
$C_{dc,af}$	DC-link capacitance of APF DC-link	F
C_f	APF ripple filter capacitance	F
C_{lisn}	LISN capacitor	F
C_{pAPF}	parasitic capacitance to ground of all floating parts of the APF	F
C_{S1}	first thermal capacitor of foster model of a switch	$J\ K^{-1}$
C_{S2}	second thermal capacitor of foster model of a switch	$J\ K^{-1}$
C_{S3}	third thermal capacitor of foster model of a switch	$J\ K^{-1}$
C_x	input filter capacitance between input phases	F
C_{xy}	sum of C_x and C_y	F
C_y	input filter capacitance against case ground	F
d_f	distance between floating parts of the APF and case	m
D_1	series diode in SiC module	

D_2	SiC free-wheeling diode in SiC module	
D_{1PLL}	damping of 6^{th} harmonic at 360 Hz by low-pass filter T_{1PLL}	
D_{2VC}	damping of low-pass filter with T_{2VC} at 60 kHz	
D_{5SSA}	damping of low-pass filter with T_{5SSA}	
D_{7SSA}	damping of low-pass filter with T_{7SSA}	
D_{900Hz}	damping of fundamental frequency at 900 Hz by low-pass filter T_{1PLL}	
D_{cc}	damping of APF current control loop	
D_{cc5SSA}	G_{cc} damping at 5^{th} harmonic	
D_{cc7SSA}	G_{cc} damping at 7^{th} harmonic	
D_{cm}	damping of CM voltage with input filter	
$D_{cm,woF}$	damping of CM voltage without input filter	
D_f	damping of differential filter	
D_i	inner core diameter of magnetic ring core	m
D_o	outer core diameter of magnetic ring core	m
D_{SSA}	damping of SSA transfer function	
E_{load}	energy which is fed into the load DC-link during one switching cycle of the APFC	J
E_{rr}	measured Err	J
E_{rr1}	approximation of E_{rr} by e-function	J
$E_{rr1,end}$	final value of E_{rr1}	
E_{rr2}	approximation of E_{rr2} by linear function	J
φ_5	phase shift of 5^{th} harmonic of phase A	rad
φ_7	phase shift of 7^{th} harmonic of phase A	rad
φ_{cc}	phase of G_{cc}	rad
φ_e	phase difference between supply and φ_{pll}	rad
f_{max}	highest relevant system frequency for control	Hz
$\hat{f}_{net}$	peak supply frequency (800 Hz)	Hz
f_{net}	supply frequency	Hz
f_{pll}	by PLL calculated supply frequency	Hz
φ_{pll}	by PLL calculated angle	rad
f_r	resonant frequency of APF ripple filter	Hz
f_{ring}	resonant frequency between L_{net} and the sum of C_f and C_{xy}	Hz
f_s	sampling frequency of basic APF control	Hz
f_{sw}	switching frequency of power electronic device	Hz
F	fringing flux factor	
G_{AD}	transfer function of analogue to digital conversion	

G_c	transfer function control block in APF current control	
G_{cc}	approximation of G_{cc2} by 1^{st} order low-pass filter	
G_{cc2}	closed-loop transfer function of APF current control	
G_{cVC}	transfer function of PID-T_1 controller	
G_f	transfer function of ripple filter	
G_{inv}	transfer function of APF inverter	
G_{lf}	transfer function of PLL loop filter	
G_p	transfer function of entire process	
G_{pVC}	transfer function of process of APF DC-link voltage control	
h_c	height of magnetic core	m
h_{cc}	step response of G_{cc}	
h_{cc2}	step response of G_{cc2}	
ϑ_{cool}	temperature of coolant during flight cycle	°C
ϑ_J	junction temperature of power semiconductor	°C
i_1	left hand input current of transfer matrix	A
i_2	right hand input current of transfer matrix	A
i_5	5^{th} harmonic in time domain	A
i_7	7^{th} harmonic in time domain	A
i_α	result of Clarke transformation of i_a, i_b and i_c	A
i_β	result of Clarke transformation of i_a, i_b and i_c	A
i_a	input current phase A of power electronic device	A
$i_{a,ref}$	reference current phase A from instantaneous power theory	A
i_b	input current phase B of power electronic device	A
$i_{b,ref}$	reference current phase B from instantaneous power theory	A
i_{B6U}	phase current into rectifier	A
i_c	input current phase C of power electronic device	A
$i_{c,ref}$	reference current phase C from instantaneous power theory	A
i_{ce}	collector current of an IGBT	A
i_{cm}	total input CM current with CM filter	A
$i_{cm,woF}$	totla input CM current without CM filter	A
i_{cm1}	CM current caused by v_{cm1} with CM filter	A
$i_{cm1,woF}$	CM current caused by v_{cm1} without CM filter	A
i_{cm2}	CM current caused by v_{cm2} with CM filter	A
$i_{cm2,woF}$	CM current caused by v_{cm2} without CM filter	A
i_{comp}	compensation current generated by APF inverter after ripple filter	A

$i_{comp,a}$	compensation current phase A	A
$i_{comp,b}$	compensation current phase B	A
$i_{comp,c}$	compensation current phase C	A
i_{comp2}	compensation current generated by APF inverter before ripple filter	A
i_{dc}	current from rectifier to DC-link capacitor	A
i_{Dr}	current through rectifier diode	A
i_{ds}	drain current of a MOSFET	A
i_f	forward current through diode	A
i_{load}	current from DC-link capacitor to load	A
i_{phase}	input phase current of power electronic device	A
$i_{phase,woF}$	input phase current without ripple filter	A
i_{ref}	reference current calculated by instantaneous power theory	A
$i_{ref,SSA}$	reference current calculated by selective signal analysis	A
i_{rr1}	time constant of E_{rr1}	s
$\hat{I}_1$	amplitude of fundamental component	A
$\hat{I}_5$	amplitude of 5^{th} harmonic current	A
$\hat{I}_7$	amplitude of 7^{th} harmonic current	A
I_{B6U}	RMS value of i_{B6U}	A
$\bar{I}_{comp}$	average absolute value of i_{comp}	A
$\hat{I}_{comp}$	peak value of i_{comp}	A
$\bar{I}_{comp}$	average absolute value of i_{comp}	A
I_{comp}	RMS value of i_{comp}	A
$\bar{I}_{cond}$	mean current through power semiconductor	A
I_{cond}	RMS current through power semiconductor	A
$\hat{I}_{dc}$	peak value of i_{dc}	A
I_{dc}	RMS value of i_{dc}	A
$\bar{I}_{Dr,sw}$	mean current for calculation of E_{rr} power loss of diode D_r	A
$\hat{I}_k$	amplitude of k^{th} harmonic current	A
I_{load}	RMS value of i_{load}	A
I_{phase}	RMS phase current after L_net	A
$\bar{I}_{sw}$	mean current for switching power loss calculation of switch	A
k_{dc}	design margin for necessary APF DC-link voltage	
k_{ipt}	IPT peak current related to I_{load}	
k	index for order of harmonic	
K_{cc}	gain of current control loop	Ω

K_{iPLL}	min. calculated integral gain of PLL loop filter	
K_{pPLL}	max. calculated gain of PLL loop filter	
K_{pVC}	gain of G_{cVC}	A
K_{SSA}	gain of 5^{th} and 7^{th} harmonic	
l_c	effective magnetic path length of magnetic core	m
l_c	effective path length of magnetic core	m
l_g	length of air gap in magnetic core	m
l_g	length of single air gap in a magnetic core	m
$l_{g,corr}$	by fringing flux corrected air gap	m
$l_{g,r}$	required length of air gap in magnetic core	m
L_a	air choke in test setup for semiconductor characterization	H
L_{APF}	total inductance relevant for APF control	H
L_b	APFC boost inductor	H
L_{cm}	CM choke in input filter	H
L_d	inductance in LCR damping circuit	H
L_{dc}	DC-link inductance	H
$L_{dc,r}$	required DC-link inductance	H
L_f	APF filter inductance	H
L_{lisn}	LISN inductor	H
L_{net}	source inductance of aircraft generator and cables	H
μ_0	absolute vacuum permeability	Vs A^{-1} m^{-1}
μ_c	relative permeability of magnetic material	
μ_{eff}	effective relative permeability of core with air gap	Vs A^{-1} m^{-1}
$\mu_{eff,r}$	required effective relative permeability	Vs A^{-1} m^{-1}
m	modulation index	
$\hat{m}$	peak value of modulation index m	
M	torque	Nm
n_1	number of windings of coil N_1	
n_2	number of windings of coil N_2	
n_3	number of windings of coil N_3	
n_r	required number of windings at inductor	
n	number of windings at inductor	
N_1	ATRU coil N_1	
N_2	ATRU coil N_2	
N_3	ATRU coil N_3	
$\hat{p}_{af}$	peak power delivered by APF DC-link	W

p_{af}	power delivered by APF DC-link	W
p_{IP}	instantaneous real power	W
$\bar{p}_{IP}$	low-pass filtered value of instantaneous real power	W
p_z	real power, which charges the APF DC-link at load dump	W
P_{APF}	total power loss of APF	W
$P_{APF,inv}$	power loss in APF inverter stage	W
P_{B6U}	power loss of rectifier diodes	W
P_{cond}	conduction power loss of power semiconductor	W
$P_{cond,D}$	conduction power loss of diode	W
$P_{cond,S}$	conduction power loss of IGBT or MOSFET	W
P_{ECS}	electrical output power of E-ECS controller	W
P_{IF}	power loss in input filter	W
P_{in}	total input power of entire power electronic device	W
P_{in2}	total input power directly before rectifier	W
P_{Ldc}	power loss in the two DC-link chokes	W
P_{Lf}	total power loss in APF filter inductors	W
P_{load}	total power of load at DC-link capacitor	W
P_{nom}	nominal output power of a power electronic device	W
P_{Rf}	total power loss in APF damping resistors	W
P_{sum}	total power loss of power semiconductor	W
$P_{sw,D}$	switching power loss of diode	W
$P_{sw,S}$	switching power loss of IGBT or MOSFET	W
P_{tot}	total power loss of entire power electronic device	W
q_{IP}	instantaneous reactive power	Var
r_{ce}	differential resistance of IGBT for approximation of conduction characteristic	Ω
r_f	differential resistance of diode for approximation of conduction characteristic	Ω
R_{APF}	total ohmic resistance for APF control	Ω
R_d	resistance in LCR damping circuit	Ω
R_{D1}	first thermal resistor of foster model of a diode	K W^{-1}
R_{D2}	second thermal resistor of foster model of a diode	K W^{-1}
R_{D3}	third thermal resistor of foster model of a diode	K W^{-1}
R_{ds}	resistance of MOSFET for approximation of conduction characteristic	Ω
R_f	APF damping resistor	Ω
R_{Goff}	gate resistor for switching-off of power semiconductor	Ω

R_{Gon}	gate resistor for switching-on of power semiconductor	Ω
R_{lisn}	LISN resistor	Ω
R_s	shunt resistor for current measurement in test setup for semiconductor characterization	Ω
R_{S1}	first thermal resistor of foster model of a switch	K W^{-1}
R_{S2}	second thermal resistor of foster model of a switch	K W^{-1}
R_{S3}	third thermal resistor of foster model of a switch	K W^{-1}
$R_{thJC,D}$	thermal resistance from junction to case of diode	K W^{-1}
$R_{thJC,S}$	thermal resistance from junction to case of IGBT or MOSFET	K W^{-1}
$R_{thJCP,D}$	total thermal resistance from junction to cooping plate of diode	K W^{-1}
$R_{thJCP,S}$	total thermal resistance from junction to cooping plate of IGBT or MOSFET	K W^{-1}
R	shunt resistor for current measurement in SiC-module	Ω
S_{in}	total input imaginary power of power electronic device	VA
S	switch in SiC-module (two MOSFET dies in parallel)	
t_{11}	first element of transfer matrix	
t_{12}	second element of transfer matrix	Ω
t_{21}	third element of transfer matrix	Ω^{-1}
t_{22}	fourth element of transfer matrix	
T_{1IP}	time constant of phase voltage low-pass filter	s
T_{1PLL}	time constant of low-pass filter at phase-to-phase voltages	s
T_{1VC}	time constant of V_{ref} low-pass filter	s
T_{2IP}	time constant of instantaneous power low-pass filter	s
T_{2PLL}	time constant of loop filter G_{lf}	s
T_{2VC}	time constant of low-pass filter of D-component in G_{cVC}	s A^{-1}
T_{5SSA}	time constant of 5_{th} harmonic low-pass filter	s
T_{7SSA}	time constant of 7_{th} harmonic low-pass filter	s
T_{cc}	time constant of G_{cc}	s
T_{cVC}	time constant of $C_{dc,af}$ model	s
T_D	necessary dead time for approximation of a digital system by a continuous transfer function	s
T_{dVC}	integral time constant of G_{cVC}	A s
T_i	integral time constant of G_{r1}	s
T_{inv}	dead time of NPT-IGBTs in APF	s
T_{iVC}	integral time constant of G_{cVC}	s A^{-1}

T_p	reciprocal value of f_{net}	s
T_s	reciprocal value of f_s	s
T_{sw}	reciprocal value of f_{sw}	s
T_t	total dead time of APF inverter	s
v_1	left hand voltage of transfer matrix	V
v_2	right hand voltage of transfer matrix	V
v_α	result of Clarke transformation of v_a, v_b and v_c	V
v_β	result of Clarke transformation of v_a, v_b and v_c	V
v_a	voltage phase A after L_{net}	V
v_{ab}	difference between v_a and v_b	V
v_{af}	output voltage of APF inverter	V
$\hat{v}_{af}$	peak value of v_{af}	V
v_b	voltage phase B after L_{net}	V
v_{bc}	difference between v_b and v_c	V
v_{boost}	switched voltage generated by APFC inverter	V
v_c	voltage phase C after L_{net}	V
v_{ca}	difference between v_c and v_a	V
v_{ce}	collector-emitter voltage of an IGBT	V
v_{cm}	CM voltage	V
v_{cm1}	CM voltage caused by load inverter	V
v_{cm2}	CM voltage caused by APFC or APF inverter	V
v_{comp}	v_{af} without input phase voltage	V
v_{dc}	DC-link voltage	V
$v_{dc,af}$	DC-link voltage of APF	V
v_{ds}	drain-source voltage of a MOSFET	V
v_f	forward voltage drop of a diode	V
v_{net}	output phase voltage of three-phase supply (before L_{net})	V
$v_{net,LL}$	phase-to-phase voltage of v_{net}	V
v_{phase}	phase voltage after L_{net}	V
v_{pp}	peak-to-peak DC-link voltage ripple	V
V_a	RMS value of v_a	V
V_{ce0}	IGBT forward voltage for approximation of conduction characteristic	V
V_{cVC}	start voltage capacitance model	V
V_{dc}	RMS value of v_{dc}	V
$V_{dc,af}$	RMS value of $v_{dc,af}$	V

$\bar{V}_{Dr,sw}$	mean blocking voltage for calculation of E_{rr} power loss of diode D_r	V
$V_{DS,rated}$	rated blocking voltage of power semiconductor	V
V_{f0}	diode forward voltage for approximation of conduction characteristic	V
$V_{GS,rated}$	rated gate voltage of power semiconductor	V
V_{N1}	RMS voltage at ATRU coil N_1	V
V_{N2}	RMS voltage at ATRU coil N_2	V
$\hat{V}_{net}$	amplitude of v_{net}	V
V_{net}	RMS value of v_{net}	V
V_{phase}	RMS value of v_{phase}	V
V_{ref}	reference voltage for APF DC-link voltage control	V
V_{ref2}	V_{ref} filtered by low-pass filter T_{1VC}	
z_{11}	first element of impedance matrix	Ω
z_{12}	second element of impedance matrix	Ω
z_{21}	third element of impedance matrix	Ω
z_{22}	fourth element of impedance matrix	Ω
$z_{11,ATRU}$	z_{11} impedance of ATRU	Ω
z_{sc}	left hand input impedance of transfer matrix at shorted right hand input	Ω
$z_{sc,ATRU}$	z_{sc} impedance of ATRU	Ω
Z_{B6U}	CM impedance matrix of rectifier	Ω
Z_{cab}	CM impedance matrix of motor cable	Ω
Z_{inv1}	CM impedance matrix of duplex load inverter	Ω
Z_{inv2}	CM impedance matrix of APFC or APF inverter	Ω
Z_{ipt}	CM impedance matrix of interphase reactor	Ω
Z_{mot}	CM impedance matrix of motor	Ω
Z_{tr}	CM impedance matrix of transformer	Ω
ω_{net}	angular frequency of three-phase supply voltage	rad s^{-1}
ω	angular frequency	rad s^{-1}

List of abbreviations

ADC analogue-digital conversion 134
APF active power filter 25
APFC active power factor correction 25
ATRU autotransformer rectifier unit 25
CAN controller area network 134
DFT digital Fourier transform 72
DMA direct memory access 135
DSP digital signal processor 118
E-ECS electrical environmental control system 25
ECS environmental control system 25
EHA electro-hydrostatic actuator 24
EOL end-of-life 60
FACTS flexible AC transmission systems 71
FFT fast Fourier transform 72
FPGA field programmable gate array 135
GTO gate turn-off thyristor 66
HVDC high voltage direct current 25
HSRF harmonic synchronous reference frame method 72
IPT interphase transformer 39
LISN line impedance stabilization network 52
MEA More Electric Aircraft 25
MOET More Open Electrical Technologies 25
McBSP multi channel buffered serial port 133
MTBF mean time between failures 34
NPT-IGBT non-punch-through-IGBT 80

PCB printed circuit board 47
POA Power Optimised Aircraft 24
PLL phase locked loop 124
PSU power supply unit 33
RAM random-access memory 134
RDM radiation design margin 66
SEB single-event burnout 68
SiC silicon carbide 69
SiFe silicon iron 39
Si-SJ silicon super-junction 69
SRF synchronous reference frame 72
SSA selective signal analysis 72
STATCOM static synchronous compensator 71
SSSC static synchronous series compensator 71
SVC static var compensator 71
UPFC unified power flow controller 71

1 Introduction

When the aircraft A320 was finished in 1987, Airbus lead the civil aviation into a new era. For the first time, hydraulic valves for the primary flight control were not controlled through bowden cables, but using electrical servo valves [1]. This technique is called "fly-by-wire", since there is no mechanical link between pilot and valves anymore. With that, the first obstacle for the step-by-step electrification was removed, which in long-term is supposed to replace all hydraulic and pneumatical systems. This trend is confirmed impressively by the significant rise of installed electrical power in current aircrafts (fig. 1.1). The predominant intention of this development is the reduction of the overall fuel consumption by lower weight. Taking a constant payload as given, the economic feasibility of an airplane increases with decreasing aircraft weight. Especially in times of rising fuel costs and fierce competition between both airlines and aircraft manufacturers, the significance of economic efficiency becomes considerable.

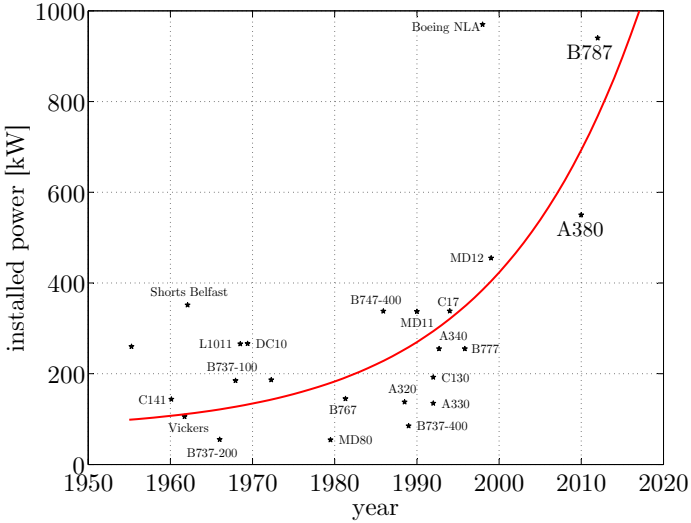


Figure 1.1: Power level increase with time (data taken from [2].)

Weight and fuel reduction are not the only reasons for the increasing number of electrical systems. Other issues are safety and flight comfort, where

the fly-by-wire technology offers further advantages. A cooperation between pilot and airborne computer is not possible in purely mechanical aircrafts. In case of a pilot failure, the computer cannot intervene and hence there is a risk of a crash. Due to the lack of mechanical rods and steel ropes of the fly-by-wire technique, the computer can influence the pilot's commands during critical flight conditions. Furthermore, the pilot can concentrate on the main manoeuvre in flight, while the computer takes care of the fine-tuning adjustment.

The fly-by-wire technique in the A320 alone is not able to arouse a significant weight reduction. Actually, the hydraulic and pneumatical systems with their long network of pipes (fig. 1.2) have the main potential. The Airbus A380 is the first aircraft, where the so-called power-by-wire technique is implemented. One of the three hydraulic pipe systems is substituted by two independent electro-hydrostatic actuators (EHAs). An EHA is an actuator, which generates the required hydraulic pressure itself using an electrical pump. The primary and secondary flight actuators are still driven by hydraulic pressure, since hydraulic systems offer the highest power density. With this configuration the A380 is still able to safely continue a flight even if both central hydraulic systems fail [1]. Other advantages of using wires instead of pipes are safety issues and lower maintenance costs. Hydraulic pipes with highly pressurized oil have leakages and are dangerous for humans in case of a failure. Future aircrafts will have no hydraulic pipe system anymore (fig. 1.3).

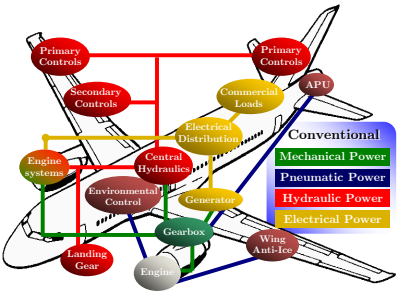


Figure 1.2: Conventional power distribution [3].

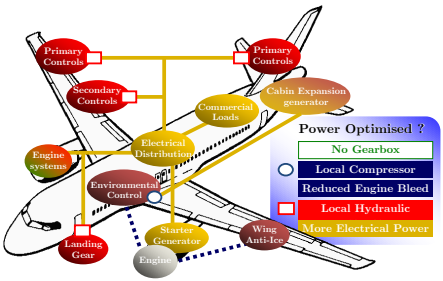


Figure 1.3: Optimized architecture in future aircrafts [3].

Energy savings are not only achieved by weight reduction, but also through intelligent control of electric actuators. The research project Power Optimised Aircraft (POA) ([3], [4], [5]), coordinated by Liebherr Aerospace in Lindenberg, evaluates the energy saving potential of different measures. In the frame of this project, the anti-icing system, which conducts hot bleed air to the wing through a network of pipes, is investigated in de-

tail. This process cannot be controlled, but only switched on and off. The application of electrical heating pads instead of bleed-air saves a lot of energy. They are switched on automatically and the output power can be controlled continuously between 0 and 100 %. Furthermore the network of pipes is no longer necessary, which reduces the overall weight.
The POA project showed that the application of electrical systems results in higher efficiency and hence lower fuel consumption. The follow-up project More Open Electrical Technologies (MOET) moves a further step and develops concrete concepts and prototypes [6], [7]). One example is the electrical environmental control system (E-ECS), which is no longer driven by bleed-air but by an electrical motor [8]. The environmental control system (ECS) regulates temperature and pressure in the cabin and is one of the biggest electrical consumers with power ratings of up to 70 kW. The first E-ECS in a commercial aircraft is integrated in the B787 from Boeing [9]. Currently, the B787 is the aircraft with the maximum expression of the More Electric Aircraft (MEA) concept, since all bleed are substituted by electrical systems except the anti-icing of the engine inlets.
In airplanes, the electrical architecture for power applications consists of a three-phase system with 115 or 230 V_{RMS} phase voltage with a variable frequency of 360 to 800 Hz. The frequency variation is caused be the generator, which is directly linked to the turbine. The turbine rotation speed is higher during take off than in the cruising altitude. All power electronic devices need a high voltage direct current (HVDC) rail, which is supplied by the three-phase system. Conventionally, the rectification of the three-phase system is performed with autotransformer rectifier units (ATRU) and active power factor correction units (APFC). Since the rectifier has the second largest portion of weight after the housing, it is worth taking a closer look to this component. This thesis investigates the active power filter (APF) as alternative to the autotransformer rectifier unit (ATRU) and the active power factor correction (APFC). The APF compensates for the 5^{th} and 7^{th} harmonics only. Due to the parallel arrangement with respect to the main power flow, the APF does not conduct the entire phase current. Hence, weight and volume are lower compared to ATRU and APFC. Furthermore, one APF can be used to compensate for the harmonics of several power electronic devices.

This thesis starts with a brief description of environmental conditions, which are important for the APF design. The next chapter evaluates the conventional rectifier topologies, which are commonly used in aircrafts. Chapter four deals with reliability and lifetime of power modules with respect to the environmental conditions of aerospace applications. The detailed design of the active power filter with semiconductor power loss

calculation and EMC issues is treated in chapter 5. The following chapter describes the control algorithm, the Simulink model and simulation results. The validation of the APF design and control algorithm is performed with a laboratory prototype and summarized in chapter 7.

2 Aerospace specific requirements

2.1 Technical data of power supply

The supply characteristics for the development of this active power filter are described in aerospace standards ABD0100 1.8 and DO160 ([10] and [11]). A summary of important parameters can be found in tab. 2.1. The typical supply in aircrafts is a three-phase sinusoidal voltage with nominal value of 230 V_{rms} (phase to neutral). The voltage varies from 216 to 236 V_{rms} in steady-state and can reach up to 360 V_{rms} in transient conditions. The source inductance L_{net} of cabling and generator is defined by

$$L_{net} = \frac{3 \cdot 0.04}{2\pi f_{net}} \cdot \frac{V_{net}^2}{P_{nom}} \tag{2.1}$$

with supply frequency f_{net}, RMS phase voltage V_{net} and nominal output power of the power electronic device P_{nom} [10]. The supply frequency is variable between 360 and 800 Hz, with slopes of up to 50 Hz/ms and 400 Hz/s. During transient operations, the compliance with the current harmonics in tab. 2.3 is not required. However, the power electronic devices must be transparent and continue operation without damage or errors.

item	value	reference
inductance of supply	refer to eq. 2.1	[10] 2.4.2.1.6.2.2
steady state input phase voltage V_{net}	216 to 236 V_{rms}	[11] 16.5.1.1.a
voltage distortion	10 %	[11] 16.5.1.8.2.
voltage asymmetry	A:238 V, B: 241 V, C: 244 V	[11] 16.5.1.1.a
transient input phase voltage	360 V_{rms} for 100 ms 296 V_{rms} for 1 s	[11] 16.5.1.1.a
steady state supply frequency f_{net}	360 to 800 Hz	[11] 16.5.1.1.a
frequency transients	400 to 440 Hz in 1 ms 400 to 350 Hz in 1 ms	[11] 16.5.1.5.2
frequency variation	+120 Hz/s from 360 to 800 Hz -400 Hz/s from 800 to 360 Hz	[11] 16.5.2.3.3
momentary power interruptions	0 to 200 ms	[11] 16.5.1.4
inrush current limitation	9 times I_{phase} up to 3 ms 4 times I_{phase} up to 500 ms 2 times I_{phase} up to 2 s	[11] 16.5.1.4

Table 2.1: Data of three-phase power supply. I_{phase} is the RMS phase current after L_{net}.

2.2 Current harmonics and EMC

The emission of conducted and radiated disturbances by power electronic devices is divided in three frequency ranges (tab. 2.2). The first range with the current harmonics in input phases are summarized in tab. 2.3. The limits are designed in such way that an application of 12-pulse rectifier is possible (fig. 2.1). The use of 6-pulse rectifiers is not possible, due to the given limits of 5^{th} and 7^{th} harmonics (refer to chapter 3.1). Tab. 2.3 defines the harmonics up to the order of 40, which corresponds to 32 kHz considering the maximum supply frequency of 800 Hz. Between the 40^{th} harmonic and 150 kHz, the current harmonics are not defined. The second range up to 100 MHz are the conducted emissions (CE), which are measured by a current transducer. The limits (fig. 2.2) are valid for common-mode (CM) and differential-mode (DM) currents. The last frequency range are the radiated emissions (RE), fig. 2.3), which are measured by an antenna.

frequency range	requirement	reference
0 to 150 kHz	current harmonics	tab. 2.3
150 kHz to 100 MHz	conducted emission (CE)	fig. 2.2
100 MHz to 6 GHz	radiated emission (RE)	fig. 2.3

Table 2.2: Definition of frequency ranges for conducted and radiated disturbances emitted by an electronic device.

number of harmonic	limit related to $\hat{I}_1$
odd harmonics 3, 5, 7	$\hat{I}_3 = \hat{I}_5 = \hat{I}_7 = 0{,}02\hat{I}_1$
odd triple harmonics k = 9, 15, 21, ..., 39	$\hat{I}_k = 0{,}1\frac{\hat{I}_1}{k}$
odd non triple harmonic 11	$\hat{I}_{11} = 0{,}1\hat{I}_1$
odd non triple harmonic 13	$\hat{I}_{13} = 0{,}08\hat{I}_1$
odd non triple harmonics 17 and 19	$\hat{I}_{17} = \hat{I}_{19} = 0{,}04\hat{I}_1$
odd non triple harmonics 23 and 25	$\hat{I}_{23} = \hat{I}_{25} = 0{,}03\hat{I}_1$
odd non triple harmonics k = 29, 31, 35, 37	$\hat{I}_k = 0{,}3\frac{\hat{I}_1}{k}$
even harmonics 2 and 4	$\hat{I}_2 = \hat{I}_4 = 0{,}01\frac{\hat{I}_1}{k}$
even harmonics > 4 (k = 6, 8, 10, ..., 40)	$\hat{I}_k = 0{,}0025\hat{I}_1$

Table 2.3: Allowed limits of harmonics in input phases currents (defined in [11] table 16-5). $\hat{I}_1$ is the amplitude of the fundamental current.

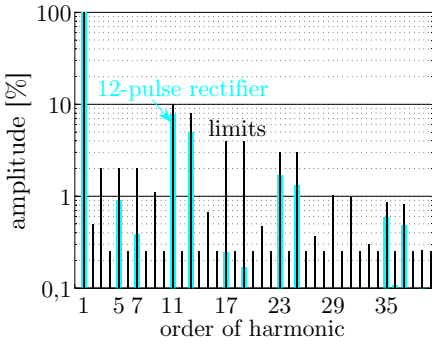


Figure 2.1: Spectrum of 12-pulse rectifier and allowed levels of tab. 2.3.

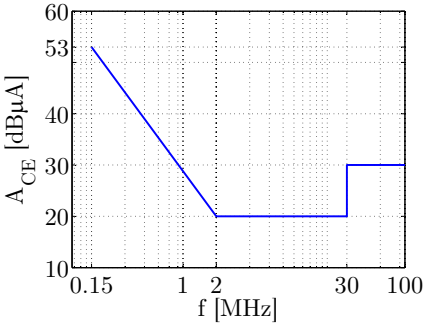


Figure 2.2: Conducted emission levels ([11] table 21-1).

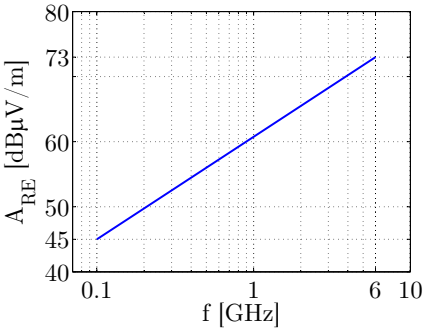


Figure 2.3: Radiated emission levels ([11] table 21-7).

2.3 DC-link voltage ripple

The DC-link voltage ripple vs. frequency (fig. 2.4) is defined in the standard MIL-STD-704 F[12]. All rectifiers must comply with these limits. The corresponding data is summarized in tab. 2.4.

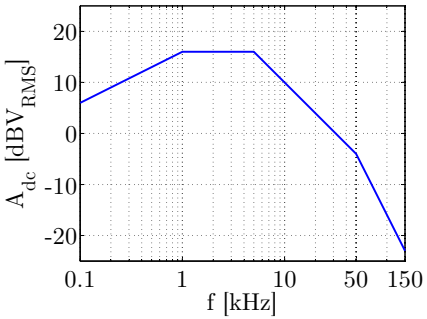


Figure 2.4: Allowed DC-link voltage ripple vs. frequency.

f [**kHz**]	$\mathbf{A_{dc}}$ [$\mathbf{dBV_{rms}}$]	$\mathbf{v_{PP}}$ [**V**]
0,1	6	5,64
1	16	17,8
5	16	17,8
50	-4	1,78
70	-9,8	0,91
150	-23	0,20

Table 2.4: Data to fig. 2.4.

The conversion from the amplitude in $\mathrm{dBV_{rms}}$ (A_{dc}) to peak-to-peak ripple voltage in V (v_{pp}) is done using

$$v_{pp} = 2\sqrt{2} \cdot 10^{\frac{A_{dc}}{20}}. \tag{2.2}$$

The intermediate value at 70 kHz is calculated through

$$A_{dc}(70kHz) = \frac{-19 \log \frac{70kHz}{50kHz}}{\log 3} - 4dBV_{rms} \approx -9.8dBV_{rms}. \tag{2.3}$$

This value is necessary for the design of the DC-link capacitance in chapter 3.3.

2.4 Load characteristic

The dynamic requirements for rectifiers in power electronic devices are not only defined by the supply. The load characteristic is an important factor, too, since the input phase currents are directly linked to the output power. All motor and load parameters can be found in [13]. The load is a compressor driven by a high-speed permanent magnet motor with a nominal rotation speed of 68000 min^{-1}. The load torque has a cubic characteristic. During start-up, motor current and torque are limited to 140 % of their steady-state values. Fig. 2.5 shows the motor and load torque, which have the same value in steady-state condition (friction is neglected in this calculation). The rotation speed and electrical power is depicted in fig. 2.6. The motor needs about 1 s until reaching the nominal rotation speed. This is not critical for a rectifier.

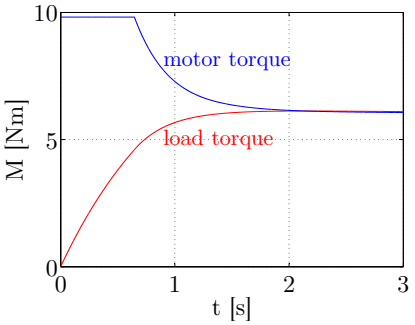


Figure 2.5: Motor load torque at motor start up.

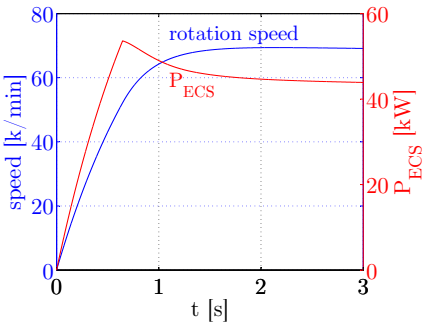


Figure 2.6: Rotation speed and electrical power during motor start-up.

The more challenging situation for a rectifier is a hard load dump. In case of a fault, the PWM signals of the motor inverter are interrupted immediately. If the rectifier is an APFC, the DC-link voltage increases due to the response time of the rectifier. If the rectifier is a diode bridge with APF, the APF DC-link increases. In both cases, the rectifier must react or switch off fast enough to avoid damages caused by too high voltages. Using an ATRU, the load dump is not critical, since there is only the remaining energy in rectifier inductances. Compared to the energy content in the DC-link capacitor, this energy is negligible.

2.5 Mission Profile

For the lifetime estimation in chapter 4.2, the characteristics of coolant temperatures [11] and E-ECS output power during one flight cycle is necessary (fig. 2.7). The E-ECS requires nominal power of 46 kW for cooling down the airplane on hot days. Once the cruising altitude is reached, the E-ECS requires maximum 30 kW for heating and pressurizing. Since the coolant is cooled by ambient air, the coolant temperature on ground is dependent on the climate, in which the airplane is operating. At cruising altitude, the coolant temperature is -9 °C, independent of the climate. The coolant is a water-glycol mixture and thus can be used at temperatures lower than 0 °C. The number of flights per day and over lifetime are depicted in tab. 2.5 [13].
The temperatures in fig. 2.7 are statistical values and valid for normal operation without failures and exceptions. They can be used for lifetime estimation only. In real applications, there are cases such as loss of cooling or extra hot day, which must be survived by the power electronic device. Hence, the relevant temperatures for the thermal design of electronic components are different (tab. 2.6).

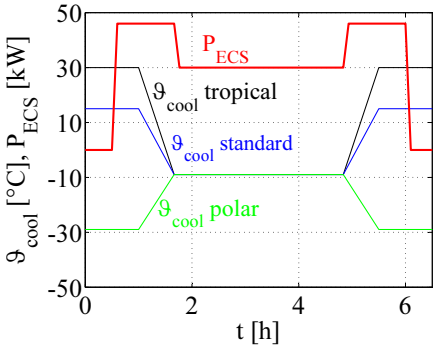


Figure 2.7: Characteristics of coolant temperatures and E-ECS output power during one flight cycle.

mission profile one flight	fig. 2.7
flights per day	4
operating days per year [d]	360
lifetime of airplane [y]	25
total flights	36000

Table 2.5: Number of flight cycles.

2.6 Minimum and maximum temperatures

The minimum ambient operating temperature is -40 °C ([11] table 4-3). This case occurs during a system start-up in polar regions. Another possible case is the start of the redundant system during flight at cruising altitude. If one PE fails, the second has to take over the function. Since the redundant system was not in duty until this time, the internal temperature can reach a minimum of -40 °C. The maximum ambient temperature inside the airplane according to [11] table 4-3 is 70 °C. This occurs at airports in hot countries. The E-ECS is cooled via a cooling plate. Considering an extra hot day with ambient air temperature outside the airplane of maximum 50 °C and a necessary $\Delta\vartheta$ between and air and coolant, the cooling plate surface reaches maximum 89 °C [13]. This is derived from a thermal FEM simulation. That is why the ambient temperature inside the PE is above 89 °C, which requires components with T_J rating of at least 105 °C.

min. ambient temperature in aircraft [°C]	-40
max. ambient temperature in aircraft [°C]	70
max. ambient temperature outside aircraft [°C]	50
max. cooling plate surface temperature [°C]	89

Table 2.6: Summary of important temperatures.

2.7 Restrictions on electrical components

Electrolytic capacitors:
In principle, the application of aluminium electrolytic capacitors in airplanes is allowed. However, an internal quality assurance instruction prohibits the application of aluminium electrolytic capacitors due to their short lifetime. They are substituted by tantalum capacitors for voltage stabilizing or energy storage applications, e.g. in power supply units (PSUs). However, tantalum capacitors are susceptible to peak currents, voltage spikes and are quite expensive. That is why the application of tantalum capacitors should be avoided whenever it is possible. An alternative for tantalum capacitors are ceramic capacitors, which are however more susceptible to mechanical vibrations and shocks.

In the DC-link of high voltage PSUs or inverters, foil capacitors are used. Foil capacitors can handle higher ripple currents due to their significantly

lower parasitic resistances. Hence, the required capacitance is lower, which partly compensates for the disadvantage of significantly lower specific capacitance ($\mu F/cm^3$) compared to electrolytic capacitors.

Optical components:
Optical components such as photo diodes, photo transistors, digital and analogue optocouplers, may be used in aircrafts. However, taking into account the mean time between failures (MTBF), which is derived from [14], optical components should be avoided. One example: a standard small signal NPN transistor at mean junction temperature of 85 °C has a failure rate of about 17 FIT (1 FIT = 1 failure in 10^9 hours). A photo transistor in the same application has 872 FIT, which is 52 times higher.

3 Rectifier topologies in aviation

3.1 Overview

Tab. 3.1 qualitatively compares the state-of-the-art rectifiers in aircrafts and the APF with each other. The topologies are evaluated from very good (++) to very bad (--). The diode bridge rectifier (B6U, fig. 3.1)

	B6U	**ATRU**	**APFC**	**APF**
power quality	--	+	++	o
weight	++	--	-	o
reliability	++	+	--	-
cost	++	o	-	--
efficiency	++	+	-	o
flexibility	--	--	--	++

Table 3.1: Qualitatively comparison of different rectifier topologies.

offers the best weight, reliability, cost and efficiency, since only six diodes are used. However, the power quality (current distortion and power factor) is the lowest. The typical phase current of a B6U is depicted in fig. 3.2 and the corresponding spectrum in fig. 3.3. The 5^{th} and 7^{th} harmonics significantly exceed the allowed level of 2 %. Hence, this topology cannot be used in aerospace applications. The APF has the highest cost due to

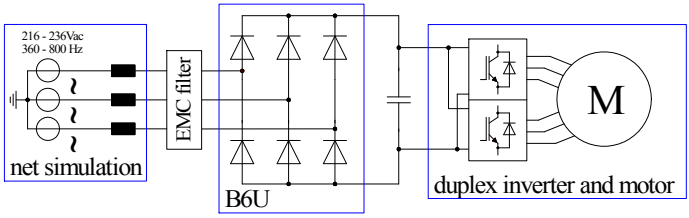


Figure 3.1: Power electronic system with diode bridge rectifier.

the required high performance of digital control but has a lower weight than ATRU and APFC. Furthermore, the APF is the most flexible topology, i.e. the APF can suppress the harmonics of several loads and can be installed retrospectively. This is required at retrofit programs, where

existing airplanes are updated with new hardware components.

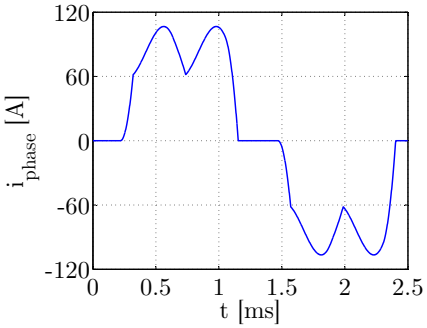


Figure 3.2: Phase current of diode bridge rectifier

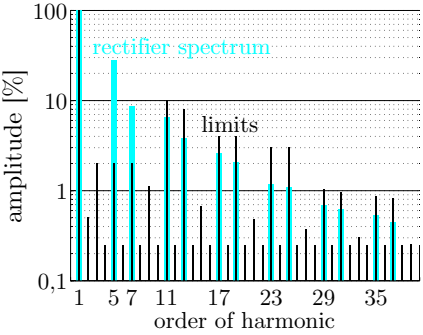


Figure 3.3: FFT analysis of rectifier current.

A possible topology with one APF and several loads is depicted in fig. 3.4. The whole network is divided into subnets while an active power filter maintains the power quality at the connection point to the main bus. Conventionally, every power electronic device at a three-phase supply requires an APFC or ATRU to be compliant with the current harmonic limits. However, the topology in fig. 3.4 allows the use of simple diode bridge rectifiers in all power electronic devices within the subnet. This increases reliability and power density while reducing costs. Since most actuators in a wing are not driven permanently and not simultaneously, the power rating of the single active power filter is significantly smaller than the total power rating of the whole subnet. Thus, the total weight of the subnet is lower, too, than applying a conventional rectifier stage in every power electronic device.

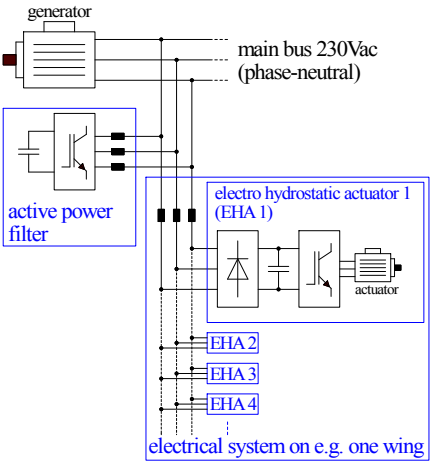


Figure 3.4: Possible subnet configuration with APF ensuring power quality at the connection point to the main bus.

A further possibility is the use of one APF with two redundant systems as shown in fig. 3.5. Only one APF is necessary, since only one E-ECS is active.

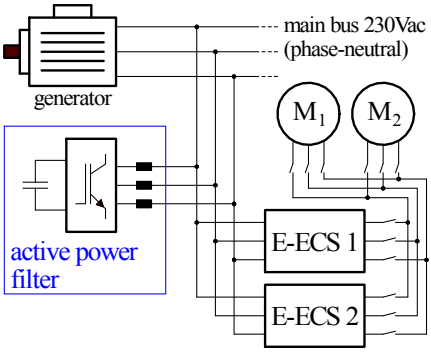


Figure 3.5: Usage of one APF with two redundant E-ECS systems.

In the following two chapters, the ATRU and APFC topologies are investigated in detail. The weight of all subcomponents is determined and summarized in tab. 3.2 and tab. 3.4. The summary of the APF weight can be found in tab. 7.4. For easy weight comparison of the three topologies, all weight values are normalized to the total ATRU weight.

3.2 12-pulse rectifier with autotransformer

3.2.1 Introduction

An ATRU consists of a 12-pulse autotransformer, two rectifiers and two interphase transformers (fig. 3.6). Employing an autotransformer instead of a conventional isolated one significantly reduces weight and volume ([15],[16]). For this reason only autotransformers are used in aerospace applications. The transformer generates two three-phase systems with a phase shift of 30°, which are rectified with standard diode rectifiers. The two DC-voltages with 6-pulse ripples are switched in parallel using two interphase transformers. The resulting DC-voltage at the main DC-link has a 12-pulse ripple.

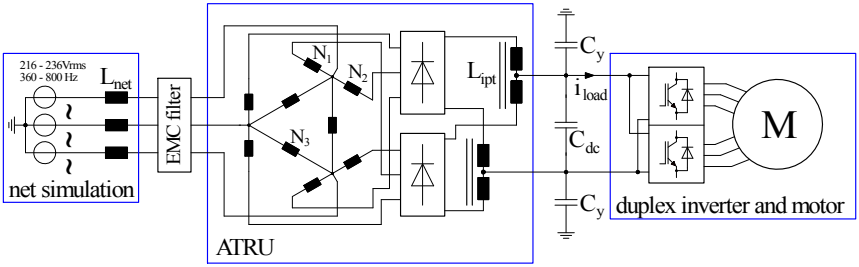


Figure 3.6: Overview ATRU with grid, source inductance, DC-link, duplex inverter and motor.

3.2.2 Design of transformer

Coils N_1 and N_2 create two phase shifted voltages with amplitudes $\hat{V}_{a1}$ and $\hat{V}_{a2}$ together with input phase voltage amplitude $\hat{V}_a$ (fig. 3.7). To achieve the 30° requirement, following relation must be fulfilled:

$$\frac{\hat{V}_{N1}}{\hat{V}_a} = \frac{\hat{V}_{N2}}{\hat{V}_a} = \tan 15° \tag{3.1}$$

with voltage amplitude $\hat{V}_{N1}$ at winding N_1 and voltage amplitude $\hat{V}_{N2}$ at winding N_2. Since N_1 and N_2 are magnetically coupled with N_3, their number of windings are depending on n_3:

$$\frac{n_1}{n_3} = \frac{n_2}{n_3} = \frac{\tan 15°}{\sqrt{3}} \tag{3.2}$$

with number of windings n_1 to n_3. To calculate n_3 the main transformer equation is used:

$$n_3 = \frac{\sqrt{2}\sqrt{3}V_a}{2\pi f_{net} B_{sat} A_c} \tag{3.3}$$

with supply frequency f_{net}, RMS phase voltage V_a, cross section of magnetic core A_c and saturation flux $B_{sat} = 1{,}6T$ considering a typical silicon iron (SiFe) core.
The RMS value of DC-link voltage can be approximated to

$$V_{dc} \approx 2{,}42V_a \tag{3.4}$$

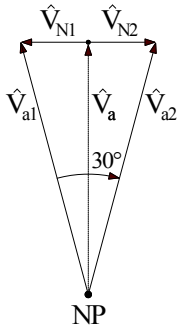


Figure 3.7: Voltage vectors resulting from N_1 and N_2.

[16]. In [15], an estimation of the RMS currents through coils N_1, N_2 and N_3 is given:

$$I_{N1} = I_{N2} \approx 0{,}4082I_{load} \tag{3.5}$$

$$I_{N3} \approx 0{,}0447I_{load} \tag{3.6}$$

where

$$I_{load} = \frac{P_{load}}{V_{dc}} \tag{3.7}$$

with RMS DC-link voltage V_{dc} and load power P_{load}. With this information, the iterative transformer design can be started. A spreadsheet (fig. 3.8) calculates necessary windings and the filling factor of the bobbin, taking into account the chosen wire configuration. Too little space on the bobbin requires the next bigger iron core.

3.2.3 Design of interphase transformers

In contrast to a conventional 12-pulse rectifier, the ATRU requires two interphase transformers (IPTs) instead of one due to the galvanically coupled three-phase systems. The design of the IPTs is not as straightforward as the transformer design. In [15], the necessary inductance L_{ipt} is estimated through

$$L_{ipt} = 0{,}1\frac{V_a^2}{f k_{ipt} P_{load}} \tag{3.8}$$

where k_{ipt} is the peak current seen by the interphase transformer related to the load current I_{load}. A reasonable range for starting first simulations is a k_{ipt} of about 40 to 50%. Since the 5^{th} harmonic mainly depends on the inductance of the interphase transformer, real measurements are im-

Transformer design 3.10

3-phase, all coils identical

Global data:				
f	360 Hz			
$B_{MAX,SOLL}$	1,6 T			
$B_{MAX,IST}$	1,29 T	P_{load} [W]	U_{phase} [V]	I_{load} [A]
$J_{MAX,SOLL}$	8 A/[mm²]	7895	115	28,36
Gesamtwickelfüllfaktor	173,66 %			
Total mass	1,88 kg	ϑ_{SOLL}	ϑ_{IST}	
Total volume	477,39 cm³	15,00	14,95	

	Primär	Sekundär			
	Wicklung 1	Wicklung 2	Wicklung 3	Wicklung 4	Wicklung 5
U_{RMS} [V] (line-line)	199	30,81	30,81		
I_{RMS} [A]	1,27	11,57	11,57		
Windings calculated	224,31	34,69	34,69		
Windings chosen	**279**	**43**	**43**		
Platzverbrauch	35%	69%	69%		
Copper length [m]	28,04	10,71	13,01		
Copper resistance [Ω]	2,462	0,059	0,071		
Copper mass [g]	49	75	91		
Current density [A/mm²]	6,5	7,4	7,4		
P_{CU} [W]	3,96	7,87	9,57		
Winding technique	Standard	Standard	Standard	Standard	

Wire data:					
Width [mm]	0,54	1,07	1,07	0,37	0,37
Height [mm]	0,54	1,07	1,07	0,37	0,37
Cross section [mm²]	0,20	0,79	0,79	0,09	0,09
Parallel wires	1	2	2	1	2
Winding data:					
Wires per layer calc.	83,3	41,7	41,7		
Wires per layer real	83	41	41		
Number of layers calc.	3,36	1,05	1,05		
Number of layers real	4	2	2		
Ausnutzung letzte Lage	36%	5%	5%		
Außenradius	2,16	6,42	10,68		

Kerndaten:	S3U 48b
a	80,8 mm
b	83,9 mm
d	25,5 mm
e	15,8 mm
f	16 mm
g	50,5 mm
r	2 mm
s	0,4 mm
L_FE	29,1 cm
A_FE	3,47 cm²
m_FE	0,776 kg
Kerntyp	S3U
Bestellnummer	54030

Spulenkörper:	UI 48b
z1	22 mm
z2	22 mm
b1	16,7 mm
b2	31,0 mm
h1	26,1 mm
h2	44,9 mm
k	9,4 mm
l1	45,5 mm
l2	47,4 mm
l3	49,5 mm
l4	53,5 mm
n1	1,0 mm
n2	0,0 mm
Wickelraumlänge	45,5 mm
Wickelraumhöhe	6,15 mm
Windungshöhe	28,1 mm
Windungsbreite	18,7 mm
Kammern	1
Art.-Nr.	151800

Constants	
μ_0	1,26E-06 Vs/Am
ρ_{CU}	1,72E-08 Ωm-1
c_{Cu}	385 J/kg/K
Copper	8930 kg/m³
SiFe	7200 kg/m³
Aluminium	2,7 g/cm³
Araldit	1,8 g/cm³
Stycast	2,45 g/cm³

Mass / volume transformer	
Mass [kg]	1,422
Volume [cm³]	252

Potting	
Length [mm]	111,80
Width [mm]	83,90
Height [mm]	44,90
Araldit	1,80
Volume [cm³]	169,36
Mass [kg]	0,305

Diode bridge current	
I_{D_AV} [A]	4,73
I_{D_RMS} [A]	8,19

Coil temperature increase	
mass per coil [kg]	0,215
copper losses [W]	21,39
duration [s]	30
ΔT entire coil [K]	7,74
ΔT hotspot [K]	8,14

Aluminium case (Becher)	
Length [mm]	115,80
Width [mm]	87,90
Height [mm]	46,90
Wall thickness [mm]	2,00
Aluminium [g/cm³]	2,70
Volume [cm³]	56,22
Mass [kg]	0,152

Figure 3.8: Extract of spreadsheet for transformer design.

portant to ensure the compliance of the ATRU with the harmonic limits. Another topic is the asymmetrical DC-current which results from small voltage differences between the two generated three phase systems. Voltage differences can be caused by differences in stray inductances and ohmic resistances between e.g. N_1 and N_2. The resulting DC voltages after the rectifier show small differences and cause DC currents, which flow through the interphase transformer. This has to be taken into account by choosing a higher saturation limit.

3.2.4 Prototype and measurements

Fig. 3.10 shows a measurement of the three-phase currents of an ATRU for aerospace application with a continuous nominal output power P_{nom}=15 kW. The corresponding harmonics spectrum is depicted in fig. 3.11. The 5^{th} and 7^{th} harmonics are significantly lower compared to the diode rectifier spectrum in fig. 3.3. The efficiency vs. normalized output power is above 97 % over a wide range (fig. 3.9). Beside robustness, this is another important advantage with respect to APFC and APF.

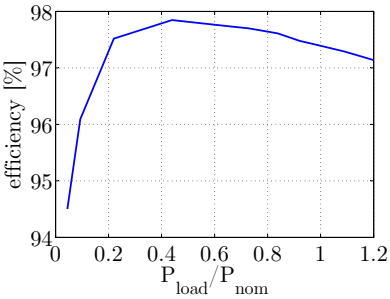


Figure 3.9: Efficiency vs. output power of the ATRU prototype with a power rating P_{nom}=15 kW (measurement).

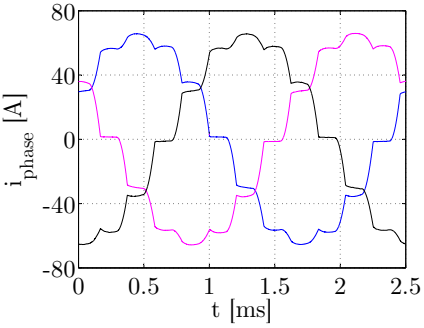


Figure 3.10: Phase currents of the ATRU prototype with a power rating of 15 kW.

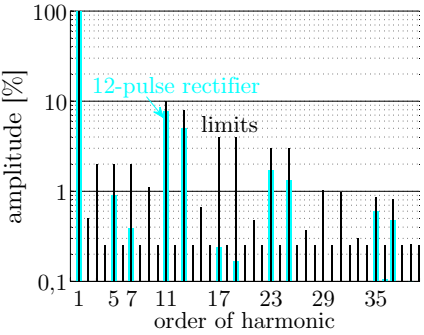


Figure 3.11: Current harmonics of phase current in fig. 3.10.

3.2.5 Design of EMC filter

The duplex inverter for the motor drive (fig. 3.6) generates differential and common-mode (CM) voltages at its output, which result in differential and CM currents at the inverter input and output. Experience shows that the differential currents are not critical, since the ATRU with interphase transformers has a stray inductance. This forms a low-pass LC-filter of high quality together with the DC-link capacitance. Furthermore, the duplex structure significantly reduces the current ripple on the DC-link due to the PWM phase shift between the two inverters [17]. That is why only the CM topic is considered in detail in the following.

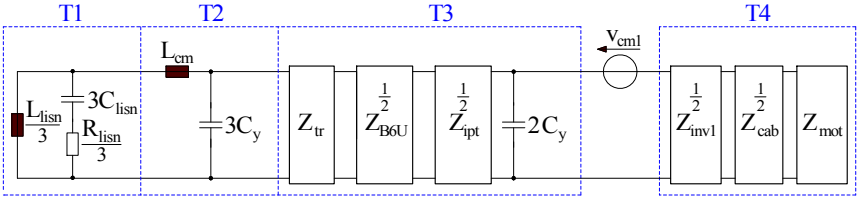


Figure 3.12: Single-phase model for CM currents, derived from fig. 3.6.

For calculating the CM currents, a single-phase model derived from the three-phase model in fig. 3.6 is necessary (fig. 3.12). From the view of a CM current, the relevant impedance is located between the three short-circuited phases to case ground. Hence, capacitances between phase and case have to multiplied by three, inductances and resistances have to be divided by three and complex impedances to case (e.g. power modules) are switched in parallel. Since all impedances are valid only for one component, a factor of $\frac{1}{2}$ is necessary to take into account two rectifiers Z_{B6U}, two interphase transformers Z_{IPT} and two power modules Z_{inv1}. Components at the three-phase system are multiplied by $\frac{1}{3}$ (L_{lisn}, R_{lisn}) or by 3 (C_{lisn}, C_y). The duplex motor inverter consists of two so-called "six-packs", i.e. one module contains a complete inverter with six IGBTs and six free-wheeling diodes. For the calculation, the duplex inverter is transformed into a single inverter by summarizing the two output CM voltages to v_{cm1}. The CM impedances of output cables and motor (Z_{cab} and Z_{mot}) are measured by an impedance analyzer. The cable is purely capacitive in the relevant range up to 10 MHz. The measurement is performed with three cables in parallel. Due to the duplex inverter, there are two three-phase systems between inverter and motor. Therefore, cable and inverter impedances are multiplied with $\frac{1}{2}$ in fig. 5.41. The motor impedance is measured with all six motor phases in parallel. Hence, factor $\frac{1}{2}$ is not necessary. The motor impedance is quite complex and cannot be modelled easily by a passive network. That is why only the dominant capacitance

is extracted.
To handle the complex single-phase model, several submodels with each a simple mathematical description as four-element matrix are defined (quadripole approach [18]). Each matrix T is defined by input and output currents and voltages according to fig. 3.13 and the following equation:

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} T \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} = \begin{bmatrix} t_{11} & t_{12} \\ t_{21} & t_{22} \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} \tag{3.9}$$

If the mathematical description of a submodel is not known, a measurement can be performed as shown in fig. 3.18 and fig. 3.20.

The parameters in matrix T are derived from the corresponding impedance matrix Z:

$$T = \begin{bmatrix} t_{11} & t_{12} \\ t_{21} & t_{22} \end{bmatrix} = f(Z) = \begin{bmatrix} \frac{z_{11}}{z_{21}} & z_{11}\frac{z_{22}}{z_{21}} - z_{21} \\ \frac{1}{z_{21}} & \frac{z_{22}}{z_{21}} \end{bmatrix} \tag{3.10}$$

Z is a four element matrix and defined by

$$Z = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}. \tag{3.11}$$

The parameters of Z are:

- z_{11}: left hand input impedance, right hand input open (fig. 3.15)
- z_{22}: right hand input impedance, left hand input open (fig. 3.16)
- z_{sc}: left hand input impedance, right hand input shorted (fig. 3.14)
- z_{12}: impedance derived from

$$z_{12} = \sqrt{z_{22}(z_{11} - z_{sc})} \tag{3.12}$$

- z_{21}: equals z_{12} for all passive systems

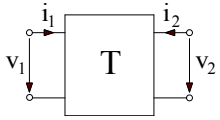


Figure 3.13: Input and output definition of one transfer matrix.

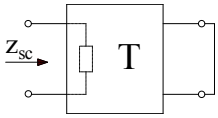


Figure 3.14: z_{sc} is defined as input impedance of left side with short circuited right side.

z_{11}, z_{22} and z_{sc} can be developed analytically if the system is known. This is demonstrated in the following example for T_2 (input filter):

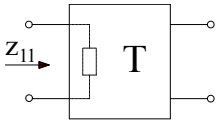


Figure 3.15: z_{11} is defined as input impedance of left side leaving open the right side.

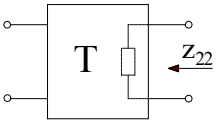


Figure 3.16: z_{22} is defined as input impedance of right side leaving open the left side.

Left hand input impedance z_{11} (right hand side open):

$$z_{11} = j\omega L_{cm} + \frac{1}{3j\omega C_y} \tag{3.13}$$

Right hand input impedance z_{22} (left hand side open):

$$z_{22} = \frac{1}{3j\omega C_y} \tag{3.14}$$

Left hand input impedance z_{sc} with shorted right hand input:

$$z_{sc} = j\omega L_{cm} \tag{3.15}$$

z_{12}, z_{21} and T are calculated using the presented formulas. Several matrices, which are connected consecutively, can be summarized by multiplication:

$$T_{sum} = T_1 T_2 T_3 ... T_n \tag{3.16}$$

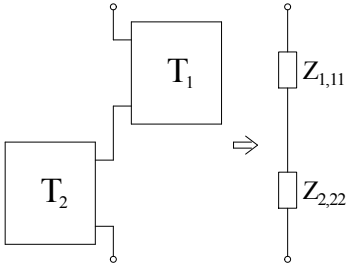


Figure 3.17: Handling of serially connected transfer matrices.

Serially connected transfer functions with one open input can be treated as two single impedances (fig. 3.17).
If the system is not known, the impedances z_{11}, z_{22} and z_{sc} can be derived from measurements. An example is shown in fig. 3.18 for z_{11} of the transformer and fig. 3.20 for z_{sc}. Both measurements can be approximated by simple passive networks (fig. 3.19 and fig. 3.21). In many cases, z_{22} is nearly identical to z_{11} and thus only two measurements need to be analysed.

For calculation of CM current, the CM voltage generated by the duplex inverter is necessary. This is generated by a Matlab calculation considering ideal switches, constant DC-link voltage of 540 V, standard PWM

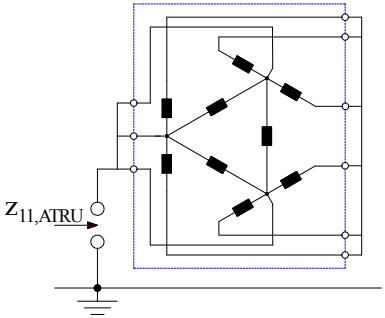


Figure 3.18: Schematic of z_{11} measurement of transformer.

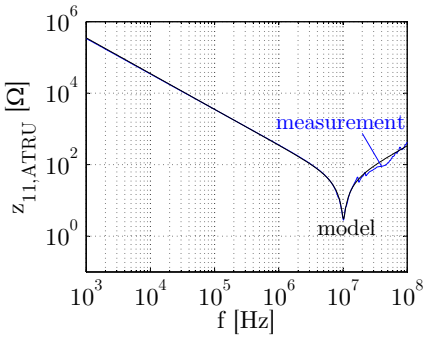


Figure 3.19: Measured and approximated z_{11} of transformer.

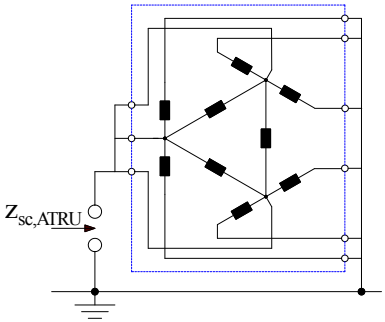


Figure 3.20: Schematic of z_{sc} measurement at transformer.

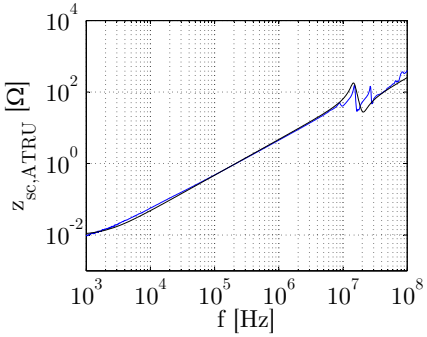


Figure 3.21: Measured and approximated z_{sc} of transformer.

(subharmonic method) and motor working point at full power. The CM voltage is depicted in fig. 3.22 (time domain) and fig. 3.23 (frequency domain). The capacitance C_y is set to the maximum possible value, which is defined in chapter 5.5.2. The resulting CM currents with and without input filter are shown in fig. 3.24. The calculation illustrates that only one CM choke is necessary for compliance with the limit. In contrast, the input filter of APFC and APF needs two CM chokes, as described in chapter 3.3.4 and chapter 5.5.2.

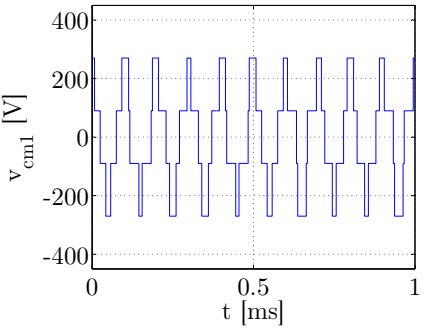


Figure 3.22: Calculated CM voltage of one inverter at output frequency of 1 kHz.

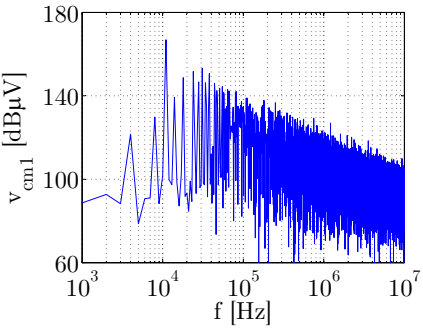


Figure 3.23: Spectrum of CM voltage in fig. 3.22.

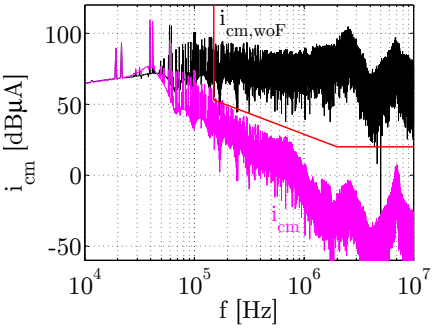


Figure 3.24: Calculated CM currents with (i_{cm}) and without input filter ($i_{cm,woF}$). The calculation is performed with CM voltage in fig. 3.23 and single-phase model in fig. 3.12.

3.2.6 Evaluation of 12-pulse rectifier

The ATRU is a very robust and reliable rectifier due to the lack of active electronic components. Only 12 diodes are necessary and optionally a temperature sensor. Furthermore, the ATRU offers a high efficiency of about 97,4 % at nominal output power. The main disadvantage is the high weight, which, however, enables a temporary overload with a multiple of the nominal power. Only the rectifiers must be adapted to withstand the temporary overcurrent. Another disadvantage is the variable DC-link voltage, which changes linearly with the three-phase input voltage amplitudes. In terms of development, qualification and production, the ATRU offers the lowest costs compared to APFC and APF. There is no control algorithm, no emission of conducted or radiated distortions, no software and no complicated stack of printed circuit boards (PCBs). However, the transformer and IPT isolation against case and the subsequent potting is quite tricky due to the high mechanical tolerances. Furthermore, the internal and external ATRU cabling causes high work load during production, since all cables must be protected and fixed to withstand the vibration level. Cabling in general is a critical topic, since manufacturing errors can easily occur. Hence, the definition and documentation of all ATRU cables must be done precisely. The weight distribution of the ATRU is summarized in tab. 3.2. All components are normalized to the total weight to simplify the weight comparison with APFC and APF. The transformer has the biggest portion with 53 % of the total weight.

transformer	0,53
interphase transformers	0,12
housing	0,07
potting	0,14
rectifier + PCBs	0,04
input filter	0,10
sum	**1,00**

Table 3.2: Weight distribution of complete ATRU.

For all applications with short power pulses, e.g. primary and secondary flight controllers, the ATRU is the favoured solution. Depending on the pulse length, the ATRU weight is 50 to 80 % lower than the result in tab. 3.2 for the same output power. Only for continuous applications such as the E-ECS, the alternative topologies APFC or APF could be considered.

3.3 Active power factor correction

3.3.1 Introduction

The active power factor correction (APFC) can be implemented using different topologies. The full bridge B6C allows power flow in both directions. Due to the prohibition of feeding back energy into the mains, this topology is not suitable for aerospace application. Furthermore, reliability is lower because a possible shoot-through of one phase-leg would short circuit the DC-link. These two disadvantages can be avoided by employing the parallel arranged six-switch rectifier (fig. 3.25) comprising bidirectional switches (fig. 3.27), which are connected in triangle (Δ) or star (Y) topology [19].

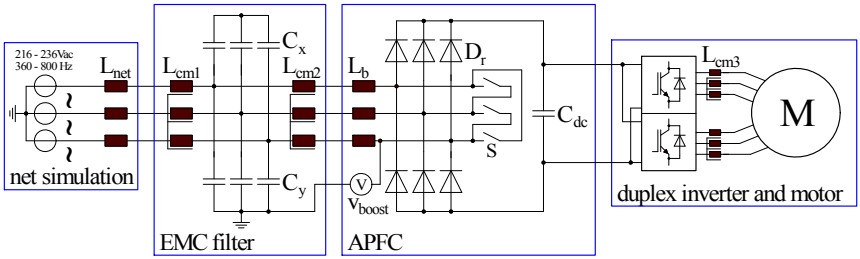


Figure 3.25: Overview of APFC with parallel connected switches in triangle topology. Bidirectional switch S is represented by a simple model. Fig. 3.27 shows a possible switch configuration.

For the calculation of semiconductor power loss, a controller based on [19] and [20] is considered. This controller can be realized by analogue circuits. The switching frequency is set to 70 kHz, which means that the second harmonic of the ripple current has a frequency of 140 kHz. As described in chapter 2.2, the current harmonics are not defined between the 40th harmonic and 150 kHz and therefore the second harmonic may have a higher amplitude than using a switching frequency of e.g. 80 kHz.

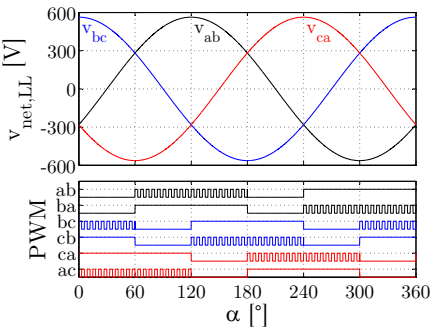


Figure 3.26: Sector dependent operation modes of the switches.

The fundamental period is divided into six sectors with each 60°. Only two switches are clocked in each sector. The third switch is not clocked, but is either continuously on (Y-topology) or off (Δ-topology). The switch

operation mode for the Δ-topology with respect to the sector is depicted in fig. 3.26. In the sector, where e.g. line-to-line voltage v_{ab} has its zero crossing, the corresponding switches S_{ab} and S_{ba} are continuously switched off. This decreases conduction power losses. That is why the Δ-topology is chosen for the further design process.

For the design of the 46 kW rectifier, the topology in fig. 3.25 with a DC-link voltage V_{dc}=700 V is chosen. The modulation index [19] is

$$m = \frac{\sqrt{3}\sqrt{2}V_{net}}{V_{dc}}. \tag{3.17}$$

The minimal value of the DC-link capacitance (eq. 3.20) is determined by the maximum allowed voltage ripple amplitude at the switching frequency, which is described in chapter 2.3. During the charging of boost inductors L_b, the DC-link must supply the motor inverter by the energy

$$E_{load} = \frac{mP_{load}}{f_{sw}} \tag{3.18}$$

with switching frequency f_{sw}. The dependency between energy and peak-to-peak DC-link voltage ripple v_{pp} is

$$E_{load} = \frac{1}{2}C_{dc}\Big[\big(V_{dc} + \frac{1}{2}v_{pp}\big)^2 - \big(V_{dc}^2 - \frac{1}{2}v_{pp}\big)^2\Big] \tag{3.19}$$

with load DC-link capacitance C_{dc} and DC-link voltage V_{dc}. Equating eq. 3.18 and eq. 3.19 and solving for C_{dc} leads to

$$C_{dc} = \frac{P_{load}m}{v_{pp}V_{dc}f_{sw}} \tag{3.20}$$

with $v_{pp} = 0{,}91V$ (tab. 2.4). Fig. 3.28 shows a phase current measurement of an APFC for aerospace application with a continuous output power of 1,5 kW and short-time power rating of 17 kW. The transition between two sectors can be seen in the phase current.

3.3.2 Power loss in semiconductor devices

The mean current $\bar{I}_{cond}$ through IGBTs S_1, S_2 and diodes D_1, D_2 is

$$\bar{I}_{cond} = \hat{I}_{phase}\Big(\frac{1}{2\pi} - \frac{m}{4\sqrt{3}}\Big) \tag{3.21}$$

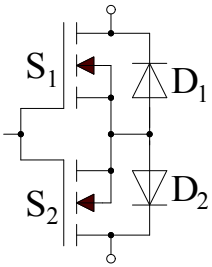


Figure 3.27: Possible configuration of switch S in fig. 3.25

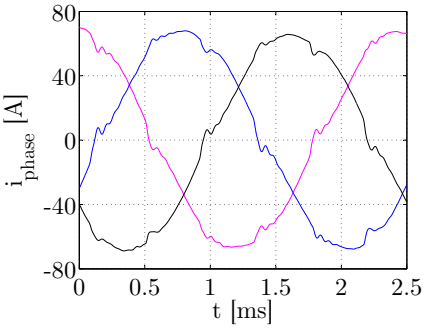


Figure 3.28: Measurement of three-phase currents of an APFC at 17 kW.

[19], where $\hat{I}_{phase}$ is the amplitude of the input phase current. The RMS current I_{cond} through IGBTs S_1, S_2 and diodes D_1, D_2 is [19]

$$I_{cond} = \hat{I}_{phase}\sqrt{\frac{1}{6} - \frac{\sqrt{3}}{8\pi} - \frac{m}{2\sqrt{3}\pi}}. \tag{3.22}$$

The mean ($\bar{I}_{cond,Dr}$) and RMS ($I_{cond,Dr}$) current through rectifier diode D_r is [19]

$$\bar{I}_{cond,Dr} = \hat{I}_{phase}\frac{m}{2\sqrt{3}} \tag{3.23}$$

and

$$I_{cond,Dr} = \hat{I}_{phase}\sqrt{\frac{m(5+2\sqrt{3})}{12\pi}}. \tag{3.24}$$

The mean current for the IGBT switching loss is derived from $\bar{I}_{cond}$:

$$\bar{I}_{S1,2,sw} = \frac{\bar{I}_{cond}}{1-m} \tag{3.25}$$

Since diodes D_1 and D_2 do not have a free-wheeling function, there is no reverse recovery. Only the conduction loss has to be taken into account. The free-wheeling path is closed by the rectifier diodes. Here, reverse recovery is present. The blocking voltage of D_r changes between $\frac{1}{2}V_{dc}$ and V_{dc} depending on the sector. On average, the blocking voltage has a value

of $\frac{2}{3}V_{dc}$, which is derived from the simulation result:

$$\bar{V}_{Dr,sw} = \frac{2}{3}V_{dc} \tag{3.26}$$

The mean current for the E_{rr} calculation $\bar{I}_{Dr,sw}$ is estimated with formula eq. 3.27. The derivation is described in the appendix (chapter A.1.1).

$$\bar{I}_{Dr,sw} = \frac{\hat{I}_{phase}}{\pi}\left(\frac{1}{\sqrt{2}} + \frac{1}{10}\right) \tag{3.27}$$

The formulas for power loss calculation of switches and diodes is described in chapter 5.4.3. Fig. 3.29 shows the normalized total losses of the Δ- and Y-topology. It can be observed that the Δ-topology offers lower power loss independent of the applied switching frequency.

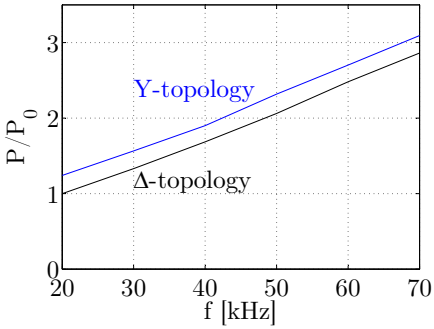


Figure 3.29: Comparison of semiconductor power loss between Δ- and Y-topology.

For the power loss calculation, the NPT-IGBT module and SiC-MOSFET module of chapter 5.4 are chosen. Their electrical parameters are summarized in tab. 5.1. The power loss results are depicted in tab. 3.3, normalized to the IGBT's switching losses. The application of SiC-MOSFET reduces the switching loss by 63 %, but increases the conduction loss by 33 %. The rectifier applies ultra fast 1200 V diodes. The reverse recovery loss is dominant and therefore the application of SiC diodes could be reasonable. However, SiC-diodes have a significantly higher forward voltage drop and therefore several SiC-diode chips should be used in parallel.

parameter	IGBT module	MOSFET module	rectifier module
$P_{sw,S}$	1,00	0,20	-
$P_{cond,S}$	0,09	0,09	-
$P_{sw,D}$	-	-	0,43
$P_{cond,D}$	0,05	0,13	0,10
P_{sum}	**1,14**	**0,43**	**0,53**

Table 3.3: Overview of rectifier and switch losses.

3.3.3 Differential mode filter design

The switched voltage v_{boost} is defined in fig. 3.25. The waveform in time domain (fig. 3.30) and the resulting spectrum (fig. 3.31) are derived by simulation and Matlab calculations. The resulting ripple current on the input phases is dependent on the ripple filter. For the first design step, the single-stage filter in fig. 3.32 is considered. Up to 150 kHz, the source impedance is modelled by the inductance L_{net} only. At frequencies above 150 kHz, L_{net} is replaced by a line impedance stabilization network (LISN) as depicted in fig. 3.33. This method is a requirement of standard DO160 ([11]). The total APFC weight is mainly determined by the boost

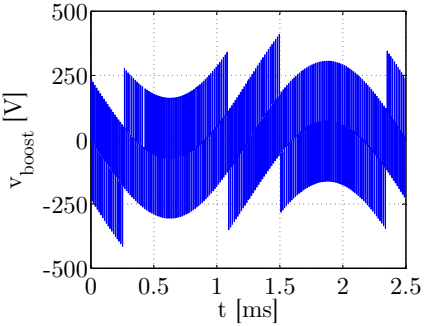


Figure 3.30: v_{boost} generated via Matlab. The switching vectors are derived from a simulation in Simulink.

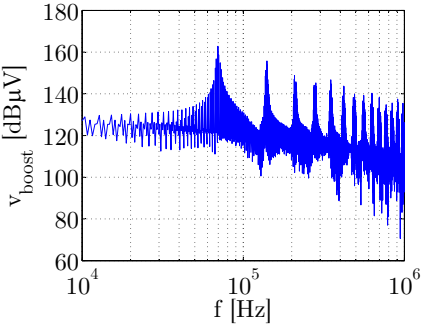


Figure 3.31: Spectrum of v_{boost} in fig. 3.30.

inductors. Hence, these inductors should be as small as possible. As shown in fig. 3.25, the source inductance is in series with the boost inductors. The ripple current is dependent on the total impedance between APFC and aerospace generator. To reduce the dependency on tolerances of the source inductance in real aircrafts, the boost inductor should have at least

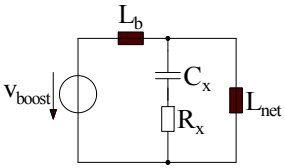


Figure 3.32: Equivalent single-phase model of one-stage ripple filter filter.

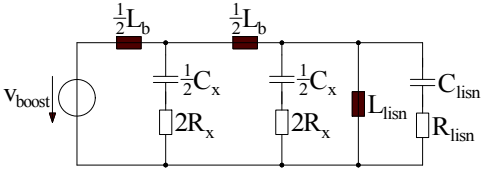


Figure 3.33: Model of two-stage ripple.

twice the value of the source inductance (eq. 2.1) as first assumption:

$$L_b = 2L_{net} \tag{3.28}$$

Another approach to deriving a reasonable value for L_b is presented in [21]. Here, a trade-off between filter capacitance, damping losses, filter damping and boost inductor value gives a similar result to the approach with twice the source inductance.

For the calculation of required filter capacitance C_x and damping resistor R_x, the transfer function of the single-stage ripple in fig. 3.32 filter is necessary:

$$G_f = \frac{sL_{net}(1 + sR_xC_x)}{s(L_b + L_{net}) + s^2R_xC_x(L_b + L_{net}) + s^3L_bL_{net}C_x} \tag{3.29}$$

The corresponding absolute damping function is

$$|D_f| = \sqrt{\frac{\Big(C_xR_x(L_b + L_{net})\Big)^2\omega^4 + \Big(L_b + L_{net} - w^2C_xL_bL_{net}\Big)^2\omega^2}{\Big(C_xR_xL_{net}\Big)^2\omega^4 + L_{net}^2\omega^2}}. \tag{3.30}$$

The resonant frequency of G_f is

$$f_{r1} = \frac{1}{2\pi\sqrt{\frac{L_bL_{net}}{L_b+L_{net}}C_x}}. \tag{3.31}$$

With the desired f_{r1}, the necessary value of C_x can be calculated. On the other hand, C_x and L_{net} form another resonant circuit with a lower resonant frequency

$$f_{r2} = \frac{1}{2\pi\sqrt{L_{net}C_x}}. \tag{3.32}$$

This resonant circuit is stimulated by voltage harmonics on the three-phase voltage, which are generated by other loads. Hence, f_{r2} should be high enough to avoid an interference with the low frequency voltage harmonics. As shown in the spectrum of 12-pulse rectifier (fig. 3.11), the 25$^{\text{th}}$ current harmonic still has an amplitude of about 1 % of the fundamental component. If a device with ATRU and a device with APFC are connected on one power bus in the aircraft, the resulting voltage harmonics will interfere with the APFC ripple filter. That is why the minimum value of f_{r2} is set to the 26$^{\text{th}}$ harmonic, which is 20.8 kHz at highest supply frequency of 800 Hz. The resulting maximum value for C_x is then

$$C_{x,max} = \frac{1}{L_{net}} \left(\frac{1}{2\pi f_{r2}} \right)^2 \approx 1.05\mu F \tag{3.33}$$

with $f_{r2} = 20.8kHz$. The subsequent minimum resonant frequency f_{r1} can be alternatively calculated to

$$f_{r1,min} = \frac{f_{r2}}{\sqrt{\frac{L_b}{L_b+L_{net}}}} = \sqrt{\frac{3}{2}} f_{r2} \approx 26.0kHz \tag{3.34}$$

with $L_b = 2L_{net}$. For the further calculations, C_x is set to 1 µF. The damping resistor R_x is defined by limiting the amplitude of G_{rf} at resonant frequency f_{r1} to 20 dB respectively damping D_{rf} to -20 dB:

$$R_x = \sqrt{\frac{\left(L_b + L_{net} - \omega_{r1}^2 C_x L_b L_{net}\right)^2 \omega_{r1}^2 - D_{rf}^2 L_{net}^2 \omega_{r1}^2}{\omega_{r1}^4 C_x^2 \left(D_{rf}^2 L_{net}^2 - (L_b + L_{net})^2\right)}} \approx 0.20\Omega \tag{3.35}$$

with $\omega_{r1} = 2\pi f_{r1}$ and $D_{rf} = -20dB$. This formula is derived from eq. 3.30. The differential mode current with the single-stage model of fig. 3.32 is depicted in fig. 3.34. Between 150 and 500 kHz, the amplitudes are not compliant with the limit. To achieve a steeper damping characteristic, a two stage filter according to fig. 3.33 is chosen. The values of L_b and C_x are divided by two. With this topology the range between 150 and 500 kHz is compliant as shown in the resulting spectrum (fig. 3.35).

3.3.4 Common mode filter design

The equivalent common-mode (CM) filter model is depicted in fig. 3.36. Two CM voltage sources are present - the boost stage of the active power

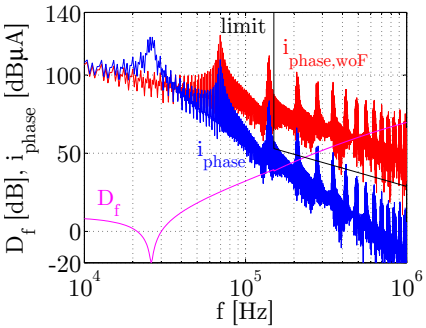


Figure 3.34: Influence of single-stage input filter (fig. 3.32) on ripple current spectrum.

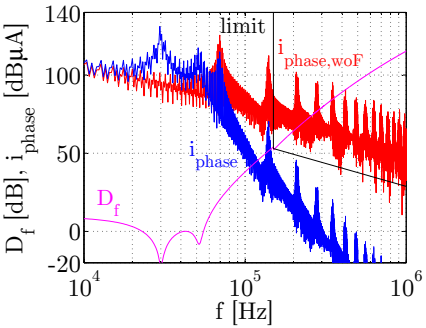


Figure 3.35: Influence of two-stage input filter (fig. 3.33) on ripple current spectrum.

factor correction (v_{cm2}) and the duplex inverter (v_{cm1}). Both voltages are calculated in Matlab. As discussed in chapter 3.2.5, the superposition principle is applied to take into account two CM voltage sources. Power module impedances Z_{inv1}, Z_{inv2}, rectifier module impedance Z_{B6U}, cable impedance Z_{cab} and motor impedance Z_{mot} are measured. An example of power module CM impedance is shown in fig. 5.44 and fig. 5.45. The APFC inverter stage consists of three power modules. They are summarized in one impedance matrix. As shown in fig. 3.25, the inverter is connected at the three-phase input only. There is no connection to the DC-link and thus the APFC inverter is only modelled by the input impedance $z_{11,inv2}$ of impedance matrix Z_{inv2}. A factor of $\frac{1}{3}$ is necessary to take into account the three existing boost modules. The duplex motor inverter, cable and motor impedance is modelled as discussed in chapter 3.2.5. The influence of input filter (T2) and output common-mode chokes L_{cm3} are depicted in fig. 3.37.

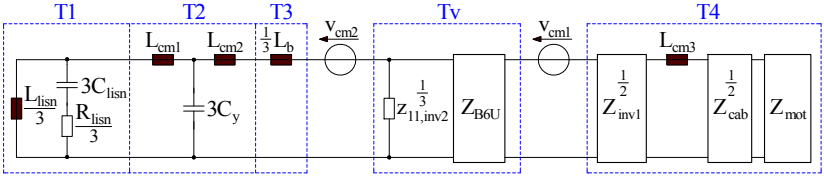


Figure 3.36: Equivalent model of fig. 3.25 for CM currents.

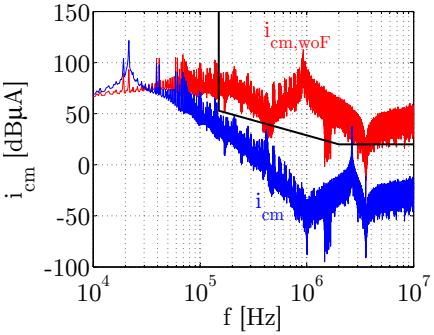


Figure 3.37: CM-current at input phases with and without input filter (output CMCs are integrated in both cases).

3.3.5 Evaluation of the APFC

The APFC offers a constant DC-link voltage, which enables an optimized motor with lower weight. A further advantage is the possibility of controlling the APFC by analogue circuits, which significantly reduces the qualification costs, since no software is necessary. However, the design and optimization of the analogue circuit must take into account all continuous and transient operations and must ensure stability over a wide temperature range.

During APFC operation, the main DC-link shows a switched CM voltage against case-ground. This means that the inverter stage, output cables and motor are switched with this CM voltage, too, which results in large CM currents. To reduce the current levels, a bigger EMC filter is necessary or additional CMCs at the inverter output have to be integrated as proposed in this APFC design. The EMC topic is the main disadvantage of the APFC.

boost inductors	0.50
input and output filter	0.21
controller board and sensors	0.05
power modules and driver boards	0.05
ripple filter	0.04
sum	**0.85**

Table 3.4: Weight distribution of complete APFC, normalized to the total ATRU weight.

The weight breakdown, normalized to the total ATRU weight, is summarized in tab. 3.4. The boost inductors cause half of the total APFC weight. In total, the APFC weight is 15 % lower compared to the ATRU.

4 Reliability of power semiconductors in aerospace applications

4.1 Statistical failures rates

A common methodology for estimating the FIT-rate of electronic components in aerospace applications is described in standard MIL-HDBK-217F [14]. The formula for power transistors takes into account constants (derived from statistical data) and the mean junction temperature:

$$\lambda = \lambda_b \cdot \pi_A \cdot \pi_Q \cdot \pi_E \cdot e^{1925\left(\frac{1}{298} - \frac{1}{\vartheta_m + 273}\right)} \cdot \frac{10^{-9}}{h} \tag{4.1}$$

with basic failure rate λ_b, mean junction temperature ϑ_m, application factor π_A, quality factor π_Q and environmental factor π_E. The number of power cycles and the corresponding temperature variations are not considered. Furthermore, this standard is from 1991 and therefore the resulting FIT-rates are too high and not applicable for current electronic devices.

Another technique for calculating FIT-rates is described in standard IEC TR 62380 [22]. The formula for power transistors is

$$\begin{aligned}\lambda = \Big[0.00275\lambda_B\big(n_1^{0.76}\Delta\vartheta_1^{0.68} + n_2^{0.76}\Delta\vartheta_2^{0.68} + n_3^{0.76}\Delta\vartheta_3^{0.68}\big) \\ + \pi_S\lambda_0\frac{\pi_{t1}\tau_1}{\tau_{on}+\tau_{off}} + \lambda_{EOS}\Big] \cdot \frac{10^{-9}}{h}\end{aligned} \tag{4.2}$$

with

$$\pi_S = \frac{V_{GS,applied}}{V_{GS,rated}} \cdot \frac{V_{DS,applied}}{V_{DS,rated}} \tag{4.3}$$

and

$$\pi_{t1} = e^{3480\cdot\left(\frac{1}{373} - \frac{1}{\vartheta_j + 273}\right)}. \tag{4.4}$$

The variables and constants of eq. 4.2 are described in tab. 4.1. Constant λ_{EOS} with a value of 40 FIT (1 FIT = 1 failure in 10^9 hours) has the main

influence on the result. This constant represents an overstress factor for the considered application. Power cycles and corresponding $\Delta\vartheta$ are dependent on the mission profile of the airplane and therefore equal for all electronic components. Furthermore, the influence of gate and drain-source voltage stress is negligibly small and power modules cannot be taken into account, i.e. only discrete components can be considered.

parameter	description
λ_0	base failure rate of die (identical for all types of switches except Gallium Arsenide switches)
ϑ_J	transistor junction temperature
τ_1	annual working rate of the equipment
τ_{on}	operating time ratio of transistor
τ_{off}	storage time ratio of transistor
n_1	annual number of first daily switch-on
n_2	annual number of switch-off between flights
n_3	annual number non-working (aircraft on ground)
$\Delta\vartheta_{1,2,3}$	temperature variation during corresponding operation
λ_B	base failure rate of transistor package
λ_{EOS}	failure rate related to the electrical overstress in the considered application
$V_{GS,applied}$	applied gate-source voltage
$V_{GS,rated}$	nominal gate-source voltage
$V_{DS,applied}$	applied drain-source voltage
$V_{DS,rated}$	nominal drain-source voltage

Table 4.1: Variables and constants used in eq. 4.2.

Both presented techniques for FIT-rate estimation are based on statistical data. They do not consider the structure of power modules and their typical failure modes. Therefore, this method is not appropriate. The evaluation of power module reliability is done in the following using the lifetime estimation, which is based on real experiments. The results are published in [23], either.

4.2 Lifetime estimation

The lifetime of power modules is limited mainly by three failure mechanisms:

- bond wire lift-off, heel crack
- degradation / delamination of chip soldering
- degradation / delamination of system soldering (solder layer between substrate and baseplate)

Bond and chip soldering failures are dependent on the number of cycles of the junction temperature ($\Delta\vartheta_J$). To determine the robustness of a power module, accelerated tests are performed in laboratory setups. The active power cycling generates a defined $\Delta\vartheta_J$ by driving a current through the collector-emitter path of an IGBT for a few seconds. This is repeated as long as no failure occurs. The cycle time should be chosen according to the real application. In [24], a calculation model based on power cycle results is presented. The number of cycles to failure N_f is calculated using a combination of Coffin-Manson law and Arrhenius equation:

$$N_f = A \cdot \Delta\vartheta_J^{\alpha} \cdot e^{\frac{Q}{R\cdot(\vartheta_m+273)}} \tag{4.5}$$

with junction temperature change $\Delta\vartheta_J$, mean junction temperature ϑ_m, $A = 640$, $\alpha = -5$, activation energy $Q = 0.8eVmol^{-1}$ and universal gas constant $R = 8.314Jmol^{-1}K^{-1}$. Since N_f is only dependent on ϑ_J and $\Delta\vartheta_J$, this model enables a simple and fast estimation of the expected lifetime. However, this model was developed using a 300A / 1200V module with one IGBT and, therefore, a transfer to other modules and type of switches is limited. Furthermore, the module structure is not taken into account.

A more detailed model for deriving N_f, taking into account the module's internal structure, is presented in [25]:

$$N_f = K \cdot \Delta\vartheta_J^{\beta_1} \cdot e^{\frac{\beta_2}{\vartheta_{J,min}+273}} \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6}. \tag{4.6}$$

with junction temperature change $\Delta\vartheta_J$, junction temperature at cycle start $\vartheta_{J,min}$, current per bond wire I, bond diameter D, blocking voltage V (divided by 100 V), cycle ON-time t_{on} (maximum 15 s), $K = 9.3 \cdot 10^{14}$ [26], $\beta_1 = -3.483$, $\beta_2 = 1917$, $\beta_3 = -0.438$, $\beta_4 = -0.717$, $\beta_5 = -0.751$ and $\beta_6 = -0.564$. This model - the CIPS 2008 model - is used for the lifetime estimation in tab. 4.3

Delamination of substrate connections is caused by solder cracks, which grow from the edge to the center of substrate. This effect is caused by temperature changes of the entire module, e.g. during changes of coolant temperature. Every temperature cycle increases the relative delamination by a certain value. On average, the delamination growth is linear and can

be expressed e.g. in 0.08 %/cycle for a Semitrans3 power module for a temperature swing between -40 and 125°C [27]. The delamination increases the thermal resistance between chip and baseplate, which results in higher chip junction temperatures with subsequent thermal chip failure. The robustness of power modules is tested using passive temperature cycles in temperature shock chambers or active heating with long power cycles. Another impact on the system solder layer is the temperature change under the chips due to the locally limited heat flow. This effect is not dependent on the coolant temperature, but dependent on the chip power loss, which heats up the ceramic. Hence, the lifetime of system solder layer is influenced by two effects: active ceramic heating and passive temperature changes.
The estimation of cycles to failure caused by active ceramic heating and passive temperature changes for a given $\Delta\vartheta_{CER}$ (CER = ceramic) is calculated using

$$N_f = N_{f,test} \cdot \left(\frac{\Delta\vartheta_{CER}}{\Delta\vartheta_{test}}\right)^{-4.5} \tag{4.7}$$

[28]. The parameters $N_{f,test}$ and $\Delta\vartheta_{test}$ are provided by the module manufacturer or derived from experiments. Own experiments with several power modules with copper and AlSiC baseplates showed that end-of-life (EOL) is not reached after 1250 passive cycles from -55 to 125 °C. That is why $N_{f,test}$ is set to 1250 and $\Delta\vartheta_{test}$ to 180 K for the following calculations. The definition of EOL is not standardized. However, several publications recommend a thermal resistance change of +20 % or a $V_{CE,sat}$ change of +5 % as failure criteria ([29], [27]).

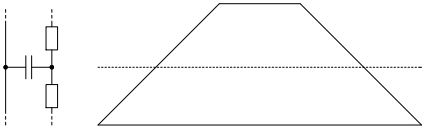


Figure 4.1: Each layer in a power module is modelled by a frustum of pyramid with two resistors and one capacitance.

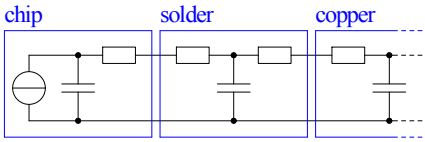


Figure 4.2: The single pyramid models are arranged in series to derive the overall Cauer thermal model.

To derive the temperatures ϑ_J and ϑ_{CER} at active operation of semiconductors, the thermal resistance of each layer in a power module has to be calculated. This approach is described in [30]. Each layer is modelled by a 45° frustum pyramid (fig. 4.1), which means that the heat flow is spread by 45°. The frustum pyramid is modelled by a Cauer model as depicted in fig. 4.2. The top and bottom part of each pyramid has a R_{th}, which

can be calculated using

$$R_{th} = \frac{l}{2\lambda A} \tag{4.8}$$

with thermal conductivity λ, total layer thickness l and area A. The thermal capacitance is caused by the volume of frustum pyramid and is derived from

$$C_{th} = Vs \tag{4.9}$$

with total volume V and thermal capacity s. All relevant material parameters can be found in tab. A.1. For example, the result of the SiC-MOSFET is summarized in tab. 4.2. The calculated junction to grease resistance $R_{th,JG}$ (layers 1 to 8) has a value of $0{,}622\frac{K}{W}$, which is not far away from the measurement in fig. 5.27 of $0.52\frac{K}{W}$. The junction to case resistance $R_{th,JC}$ with $0{,}275\frac{K}{W}$ is lower than the specified value in the datasheet[1] ($0.43\frac{K}{W}$). This difference can be eliminated with a heat flow spreading of 23° instead of 45°. However, the subsequent value for $R_{th,JG}$ is then $1.26\frac{K}{W}$, which is significantly above the measurement result. That is why the value for $R_{th,JC}$ is taken from the datasheet. For the calculation of active cycles, the total thermal resistance $R_{th,tot}$ between junction and cooling plate (CP) is necessary:

$$R_{th,tot} = R_{th,JC} + R_{th,G} + R_{th,CP} \tag{4.10}$$

with $R_{th,JC} = 0{,}43\frac{K}{W}$, $R_{th,G} = 0{,}347\frac{K}{W}$ and $R_{th,CP} = 0.082\frac{K}{W}$ (for the SiC-MOSFETs). The thermal resistance for the other components (diodes, NPT-IGBT) are derived by the same approach. For the active ceramic heating, the thermal resistance from ceramic to cooling plate is necessary. Since the thermal resistance from chip to ceramic is negligibly small compared to the total resistance, $R_{th,tot}$ is used for the calculation of ceramic temperature, too.

The mission profile with coolant temperature $\vartheta_{cool}(t)$ and required output power of the E-ECS is described in chapter 2.5. The calculated semiconductor power loss P_{loss} can be found in chapter 5.4.3. The absolute junction temperature ϑ_J is then defined by

$$\vartheta_J(t) = \vartheta_{CER}(t) = \vartheta_{cool}(t) + R_{th,tot}P_{loss}(t) \tag{4.11}$$

with $R_{th,tot}$ according to eq. 4.10 and total chip power loss $P_{loss}(t)$. The ceramic temperature $\vartheta_{CER}(t)$ is equal to $\vartheta_J(t)$, since the same thermal resistance is used. The resulting $\vartheta_J(t)$ for the three different coolant temperature profiles are depicted in fig. 4.3. To simplify the extraction of

[1] Microsemi confirmed that the thermal resistance in the datasheets are theoretical values calculated without any heat spreading.

no.	layer	material	thickness [mm]	R_{th} [K/W]
1	chip (J)	SiC 4H	0,39	0,016
2	solder 1	PbSnAg	0,10	0,036
3	copper 1	Cu	0,30	0,017
4	ceramic (CER)	AlN	0,64	0,060
5	copper 2	Cu	0,30	0,010
6	solder 2	PbSnAg	0,20	0,034
7	base plate	AlSiC	3,00	0,102
8	thermal grease (G)	grease	0,05	0,347
9	cooling plate (CP)	Al	10,0	0,082
total				**0,704**
$R_{th,JC}$ (layers 1 to 7)				0,275
$R_{th,JG}$ (layers 1 to 8)				0,622

Table 4.2: Calculation of R_{th} of each layer in the SiC-MOSFET power module.

temperature cycles using the rainflow method [31], the temperatures vs. time are transferred in peak graphs (fig. 4.4).

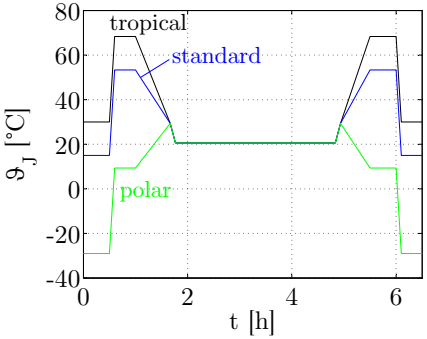


Figure 4.3: ϑ_J at different coolant temperatures during one flight cycle.

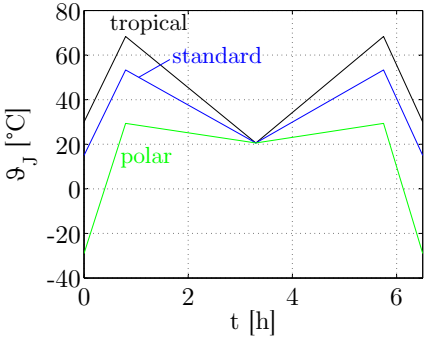


Figure 4.4: ϑ_J transformed into peak graphs.

Only MOSFET and IGBT are taken into account in the following cycle calculation, since the free-wheeling diodes have lower power losses and temperatures. The worst case for the junction temperature is the tropical profile and for the active ceramic heating the polar profile. This difference is due to the cycle start temperature $\vartheta_{J,min}$, which is taken into account by the active cycles equation only. The passive ceramic temperature (without

power loss in chips) is equal to the coolant temperature. Here, the tropical profile is the worst case, since the coolant temperature drops from 30 to -9 °C. This profile corresponds to one passive cycle only.
The results with temperatures and corresponding cycles to failure are summarized in tab. 4.3 (active cycles) and tab. 4.4 (active ceramic heating and passive cycles). Considering e.g. active cycle 1 of the SiC-MOSFET, which has a $|\Delta\vartheta_J|$ of 38,3 K and a $\vartheta_{J,min}$ of 30 °C, the resulting active cycles to failure are 1,6e^9. The lifetime consumption is then calculated taking into account the total cycles of 36000, which occur during the entire life of the aircraft (tab. 2.5). The lifetime calculation shows that only the system soldering has a significant impact on the power module lifetime. The IGBT has the maximum lifetime consumption with 32,2 %, which is not critical considering the applied worst case of temperatures and thermal impedances. Since the E-ECS is switched on once per day, the consumption caused by active cycles is very low and is nearly negligible.
The CIPS 2008 model (eq. 4.6) was developed for IGBTs with standard solder and aluminium bonds. The application of copper bonds, bondless chip connections ([32], [33]) or sintering technology [34] has a significant impact on the number of cycles to failure. In these cases the lifetime cannot be estimated with the CIPS 2008 model or the result has to be scaled in a reasonable manner. Furthermore, this model does not take into account the mechanical properties of SiC. SiC has a four times higher thermal conductivity and three times higher Young's modulus compared to silicon. This leads to the assumption that the lifetime is lower compared to an IGBT in the same housing. This assumption is confirmed by simulations with finite element method [35] and experiments. First power cycle results show that SiC devices have only about 30 % of the power cycling capability of Si-IGBTs in the same housing [36]. Due to small size of SiC chips, the solder crack growth causes a critical thermal resistance increase at lower number of cycles than using a bigger IGBT chip. To take into account the model uncertainties and the new power cycle results, the values of lifetime consumption through active cycles are multiplied by 10.

	$\lvert\Delta\vartheta_J\rvert$ [K]	$\vartheta_{J,min}$ [°C]	N_f	lifetime consumption [%]
SiC-MOSFET module				
cycle 1	38,3	30,0	1,6E+09	0,022 (10*0,0022)
cycle 2	47,8	20,6	9,3E+08	0,039 (10*0,0039)
total				**0,061**
NPT-IGBT module				
cycle 1	46,9	30,0	1,3E+09	0,003
cycle 2	48,5	28,4	1,2E+09	0,003
total				**0,006**

Table 4.3: Lifetime consumption through active power cycles (eq. 4.6).

	$\lvert\Delta\vartheta_{CER}\rvert$ [K]	N_f	lifetime consumption [%]
SiC-MOSFET module			
cycle 1 (active ceramic heating)	58,3	2,3E+05	16,0
cycle 2 (active ceramic heating)	8,8	1,1E+09	0,00
passive cycle	39,0	1,4E+06	2,61
total			**18,6**
NPT-IGBT module			
cycle 1 (active ceramic heating)	66,9	1,2E+05	29,6
cycle 2 (active ceramic heating)	9,5	7,9E+08	0,00
passive cycle	39,0	1,4E+06	2,61
total			**32,2**

Table 4.4: Lifetime consumption through active ceramic heating and passive temperature changes (eq. 4.7).

4.3 Cosmic radiation

Cosmic radiation was discovered by Victor Francis Hess in 1912 [37]. He made several trips with free balloons, where he noticed an increase in γ-radiation at altitudes above 3000 m. Since the γ-radiation from radioac-

tive material in the earth's crust decreases to about 10 % at an altitude of 500 m, the radiation at 3000 m must have its origin in space. This is not entirely correct as we know in the meantime. Isotropic primary cosmic particles with high energy (mostly protons) penetrate the earth's atmosphere and interact with atoms. These collisions cause showers of particles, which are called cosmic rays / radiation [38] (secondary radiation). The influence of cosmic radiation on low power signal electronics was already investigated in 1979 by Ziegler and Lanford [38]. Especially in the computer industry, unexplained events and spontaneously changes of digits were known as "soft fails", which are caused by cosmic particles among others. Since 1994 it is evident that power semiconductor devices are susceptible to cosmic rays, too ([39], [40], [41]). Experiments in a salt mine 140 m below ground proved that only cosmic radiation causes the failures, which occur in the laboratory outside the salt mine [39]. The characteristics of terrestrial cosmic radiation are described in [42] and [43]. Experiments in 400 m and 2964 m altitude ([44]) confirm the increase of nucleon flux as predicted in [43].
Considering a FIT-rate of 100, one device under test (DUT) would have one failure in 1141 years. To reduce the testing time to an acceptable value, several 100 devices are necessary. A further acceleration can be achieved by moving the test setup to high mountains such as Zugspitze (2964 m) or Jungfraujoch (3580 m). However, the most comfortable way of FIT-rate determination is the irradiation with nucleons using an artificial source. One source, which is able to deliver a similar neutron flux characteristic up to 800 MeV, is the neutron beam at Los Alamos Neutron Science Center (LANSCE) [45]. The natural flux shows neutrons with energies up to 6000 MeV [45]. However, a comparison between artificial neutron beam tests and natural tests on mountains shows that the high energetic neutrons are dispensable [46]. Furthermore, neutrons and protons are responsible for the majority of failures. Other particles such as myons and pions are negligible [44].
Neutrons are identified as main cause for device failures, which however does not explain the failure mechanism itself. A possible mechanism is a nuclear reaction between a neutron and a silicon nucleus in the semiconductor. This collision generates ions, which initiate a highly localized, highly concentrated charge plasma. If the device is reverse biased, the plasma can be amplified (avalanche multiplication) and develops from the anode to the cathode. This effect is called "streamer" [47]. The streamer short-circuits the device for about 20 ns. The temperature distribution can be derived from electro-thermally coupled simulations. The results give an explanation for the thermal breakdown ([48], [49]).

The SEB triggered failure mechanism in SiC-diodes is investigated in [50]. The drift region of SiC power devices can be reduced to one-tenth compared to Si devices. This results in a 10 times higher peak electrical field strength and subsequently to a 100 times higher heat generation density. Hence, the increase of lattice temperature is 100 times faster then in Si devices. This could lead to very high lattice temperatures, which can reach sublimation temperature. Experiments with a white neutron irradiation confirmed the presence of very high temperatures after a neutron impact. The surface has crown-shaped aluminium and the lattice has cracks inside the device due to expansion stress. To conclude, SiC power diodes show a similar failure mechanism compared to Si diodes, but the destruction can be significantly larger due to the higher electric field.

One possible way to reduce the failures induced by cosmic radiation is shielding. As shown in experiments with GTOs [51], the FIT-rates could be reduced by nearly factor 10 using a concrete shielding of 50 cm. In [52] the shielding performance of different materials is simulated and evaluated. Iron and lead show a significantly higher shielding performance than hydrogenous materials polyethylene and water. Especially for neutrons with energies above 20 MeV, iron turns out to be the best shielding material. However, considering an iron thickness of 10 cm, the neutrons with more than 20 MeV are reduced only by about 40 %, neutrons with lower energy are even amplified by the generation of secondary neutrons. It can be concluded that shielding is not reasonable for the majority of applications due to the high weight and low shielding effect.

In [53] the cosmic radiation is taken into account with radiation design margins (RDMs), which are defined by the customer and have to be validated during the qualification process. The RDM has to be chosen in such a way that both cumulative and single-event effects (destructive and non-destructive) are covered. To apply this approach the acceptable radiation dose for the components of interest and a model describing the real occurring dose are required. Since neither information is available yet, this approach is currently not followed.

A model for the prediction of failure rates caused by cosmic radiation was developed by H. R. Zeller in 1995 [41]. This model considers physical parameters such as device area, n-base thickness, n-base resistivity, applied voltage and device internal electrical fields. The model verification is done with diodes, thyristors and gate turn-off thyristors (GTOs) with voltage ratings from 2000 to 9000 V from different manufacturers [54]. There is no correlation between device type and manufacturer. The model is based on two important assumptions:

- the total failure rate is the integral over the local failure rate
- the electrical field is a linear function

In IGBTs, there are local field peaks close to the cathode, which are dependent on the detailed form of cathode design. An analytical description of the failure rate is not possible and therefore this developed model cannot be applied to IGBTs. A numerical calculation for a high voltage IGBT exhibits that the failure rate of an IGBT is about 10 times above the failure rate of a GTO. This is confirmed by experimental data on IGBTs [54]. These publications show that the device type and the internal field distribution have a big impact on the failure rates induced by cosmic radiation.

The reason for the higher failure rates of IGBTs is not only presence of field peaks. In [44] it is assumed that IGBTs are more susceptible to cosmic rays, since they have an intrinsic parasitic thyristor. This thyristor can latch-up and therefore generate a positive feedback, which further amplifies the collector current. In [55], the higher susceptibility of IGBTs is proven by experiments and simulation.

A comparison between the Zeller model in [41] and accelerated measurements at 1700 V diodes is presented in [56]. The proton flux I_0 is 7,39e^4 p/(cm^{2}s) at 1600 and 1700 V. With lower voltages, the flux is increased up to 250*I_0 to achieve a device failure during an acceptable testing time. Between 1400 and 1500 V, the difference between model and measurement is several orders of magnitudes (fig. 4.5). Even with the correction factor of Pfirsch in [57], the prediction at lower voltages is not acceptable. Futhermore, the FIT-rate with natural radiation is 8 to 12 times higher. The used proton beam with 200 MeV seems to be not optimal for reproducing the natural conditions [56]. This publication shows that the explanatory power of models for FIT-rate prediction is limited. The results must be interpreted very carefully. The real FIT-rate is strongly dependent on many parameters such as device type, internal device design, applied voltage, radiation type and radiation source.

An empirical model based on measurements is described in [58]. The resulting formula depends on the type of IGBT module, altitude and junction temperature. For module 5SNA1600N170100 from ABB, 10 km altitude and 125 °C junction temperature, the resulting formula is

$$\lambda\Big(\frac{V_{dc}}{V_{rated}}\Big) = 6.5 \cdot 10^7 e^{\frac{0.54}{0.58-\frac{V_{dc}}{V_{rated}}}} \tag{4.12}$$

with applied voltage V_{dc} and rated voltage V_{rated}. Fig. 4.6 depicts eq. 4.12 as diagram. However, this formula is valid only for the described

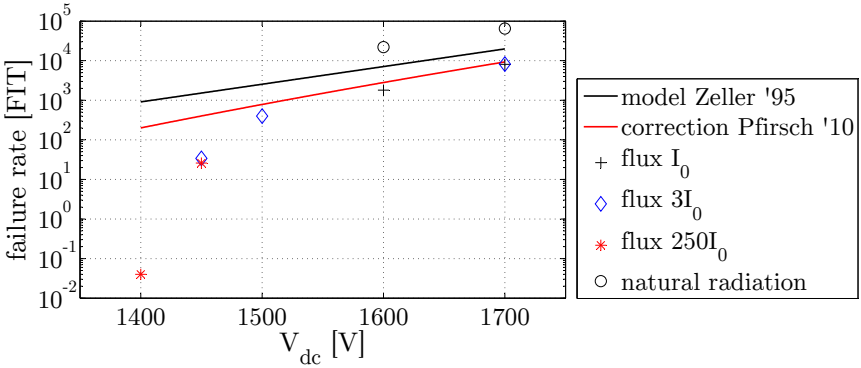


Figure 4.5: Prediction and measurement of FIT-rates induced by cosmic radiation (data taken from [56]).

IGBT modules in [58].

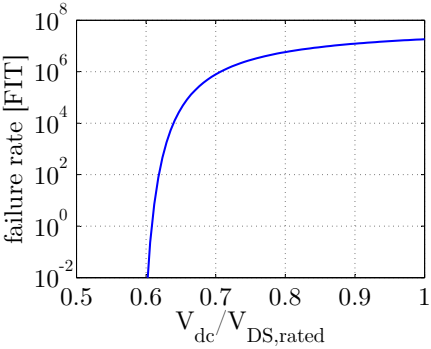


Figure 4.6: FIT-rate according to eq. 4.12.

SiC components are expected to offer a better ruggedness against cosmic radiation due to the wider band gap, the higher breakdown field and higher melting point [59]. Experiments with SiC-JFETs prove the superior ruggedness and makes SiC the preferred material for high radiation environments such as nuclear power applications ([60], [61]). Even with a neutron fluence of 10^{15} n/cm^2, no significant degradation could be found. The neutron hardness can be further improved by higher doping of the SiC device [62]. This is possible due to the 10 times higher breakdown voltage than silicon. However, these experiments do not consider single-event burnouts (SEBs) during reverse-biased operation, where the internal electric field strengths are higher than in silicon. Basically, a carrier multiplication and generation of streamer is therefore possible, too. Experiments with reverse-biased SiC-diodes show that a SEB-like event can be caused by a combination of lattice defects and a proton impact [63]. The defects can be radiation displacement damages and material defects such as clusters, screw defects, micropipes or stacking faults. Even with a low radiation, a breakdown cannot be excluded, if there are enough material defects.

Experiments with 600 and 1200 V silicon and silicon carbide (SiC) diodes exhibit heterogeneous results [64]. As expected, the 1200 V components showed a significantly higher radiation hardness than the corresponding silicon devices. However, the behaviour of the 600 V diodes was vice versa. Here, the silicon devices had lower FIT-rates.
The SiC-MOSFET manufacturer Rohm conducted an irradiation test with five 1200 V SiC-MOSFETs at 840 V DC-link voltage [65]. The fluence was $1.87 \cdot 10^9$ n/cm^2, generated with a white neutron beam (1 to 400 MeV). No MOSFET failed. However, the duration of this test is not denoted and five samples is not enough to achieve a reasonable statistical result.
Another irradiation test with three silicon super-junction (Si-SJ) MOSFETs, one 1200 V NPT-IGBT and one 1200 V SiC-MOSFET conducted at two neutron beams ($1.5 \cdot 10^4$ n/(cm^{2}s) at 50 MeV and $5.7 \cdot 10^4$ n/(cm^{2}s) at 80 MeV) is presented in [66]. Up to the maximum applied voltage of 950 V, the SiC-MOSFET does not show any failure. The failure threshold of the NPT-IGBT is at 750 V, which is 62.5 % related to the rated voltage of 1200 V. This result is quite similar to the calculated FIT-rate with eq. 4.12. Here the threshold is at approximately 60 %. The lowest threshold has a Si-SJ MOSFET with 52 %, i.e. the design in the application should take into account a derating of 48 %.

There is a trend that SiC devices offer a higher ruggedness against cosmic radiation. However, further investigations and field experience in industry applications is necessary, until SiC components can be used in aircrafts. In this work, 1700 V SiC-MOSFETs and diodes are chosen to further increase the cosmic radiation ruggedness. The power loss difference between 1700 V and 1200 V SiC-MOSFETs is significantly lower than between 1700 V and 1200 V IGBTs. Hence, the use of 1700 V SiC-MOSFETs increases the overall power loss only marginal.

5 Design of parallel active power filter

5.1 State-of-the-art active power filters

For decades, flexible AC transmission systems (FACTS) have been used in power distribution systems for voltage stabilizing, reactive power compensation and power flow control. An overview and the definition of the different types of active and passive FACTS devices is presented in [67] and [68]. There are e.g. thyristor-switched static var compensators (SVCs) with several 100 MVar [69], IGBT-switched static synchronous compensators (STATCOMs) with up to 32 MVar [70], static synchronous series compensators (SSSCs) [71]) or unified power flow controllers (UPFCs), which is a combination of STATCOM and a SSSC [72]. With the introduction of the IGBT and rising calculation power of signal processors, active harmonic power filters are becoming interesting. They can typically compensate for distorted currents or voltages up to the 50^{th} harmonic. Commercially available are e.g. cascadable harmonic filter modules with compensation currents up to 300 A [73], which equates about 800 kW load power.

There are various techniques for controlling active FACTS and power filters, which all have one basic structure: a reference generation and an error amplifier. The most important reference generation technique for active filters is the instantaneous power theory ([74–76]). This approach uses the three-phase currents and voltages for calculating the total real and imaginary power (p and q). With low-pass filtered power and phase voltages, the sinusoidal phase current can be derived. The instantaneous power theory does not need any line synchronization components, which makes it extremely robust. However, the quality of the calculated reference current is directly linked to the quality of phase voltage. There are three basic possibilities of calculating the reference current: by assuming equal power, equal current or equal resistance for each phase ([77–79]). If the three-phase system is unbalanced, it is necessary to adjust the reference calculation according to the application.

Since the quality of calculated reference current is not sufficient in some applications, the phase voltage is substituted by an artificially calculated sine signal. This approach is called synchronous reference frame (SRF) ([80–83]). A synchronization with the supply voltage is necessary and therefore the robustness is lower compared to the original instantaneous power theory. Depending on the low-pass filter of d and q, it is possible to achieve a nearly perfect sinusoidal reference current, which is independent on the phase voltage waveform.
The SRF method can be extended by a further rotating frame, which has e.g. the frequency of the 5^{th} harmonic. This so-called harmonic synchronous reference frame method (HSRF) enables the extraction of amplitude and phase of voltage or current harmonics ([84–87]). The HSRF method is suited for three-phase systems only. For single-phase systems, the selective signal analysis (SSA) can be applied as described in [88].
A further possibility of harmonics extraction are frequency-domain methods such as digital Fourier transform (DFT) ([89, 90]), fast Fourier transform (FFT) [91] and recursive DFT ([92, 93]). With the growing performance of digital signal processors (DSP), these methods can be applied in real-time systems depending on the available calculation time.

The referenced publications so far all deal with active filters for 50 / 60 Hz industrial applications. There are only few papers, which focus on active filters for aerospace applications ([94–103]). Most of these publications are not applicable to this work, since the power ratings are significantly lower and the power density is not taken into account.

The choice and design of control algorithm for this work is described in the following chapters and published in [104] and [105].

5.2 Requirements and system analysis

The concept and prototyping of the proposed APF is published in [106]. The parallel APF is integrated into a housing together with the diode rectifier and DC/AC inverter. Fig. 5.1 shows an overview of the entire system consisting of grid, non-linear load and APF. The inductors L_{net} represent the generator and cable inductance and L_{dc} the additional inductors for decoupling of APF and load. The design of L_{dc} is described in chapter 5.3.

Fig. 3.2 shows a typical waveform of a diode bridge rectifier and fig. 3.3 the corresponding harmonics spectrum. Only the 5^{th} and 7^{th} harmonic

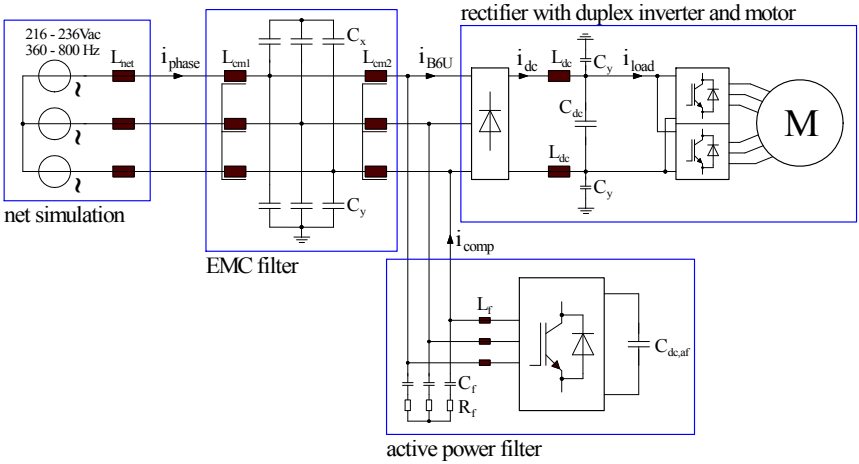


Figure 5.1: System overview with net simulation, EMC filter, rectifier with load and active power filter.

exceed the limits defined in [11] and must be compensated for. With a maximum supply frequency $\hat{f}_{\text{net}} = 800Hz$ and a PWM clock to signal frequency ratio r=10 as a common approach, the switching frequency of the active filter must be at least

$$f_{sw} = 7r\hat{f}_{net} = 56kHz. \tag{5.1}$$

The chosen switching frequency in simulations and prototype is set to 60 kHz. The resulting current ripple is damped by a filter, which is described in chapter 5.5.1. However, the filter inductor L_f is limited by the maximum voltage at $C_{dc,af}$, which is derived in the following. Considering only the main components 5^{th} and 7^{th} harmonics, the compensation current can be defined by

$$i_{comp}(t) = \hat{I}_5 sin(5\omega_{net}t + \varphi_5) + \hat{I}_7 sin(7\omega_{net}t + \varphi_7), \tag{5.2}$$

with

$$\omega_{net} = 2\pi f_{net} \tag{5.3}$$

(fig. 5.2). Parameters $\hat{I}_5$ and φ_5 are amplitude and phase of the 5^{th} harmonic, $\hat{I}_7$ and φ_7 are amplitude and phase of the 7^{th} harmonic . The necessary compensation voltage is determined mainly by L_f, since the other ripple filter components have nearly no influence at low frequencies. L_{dc} and C_{dc} are neglected, too, because one phase conducts current only

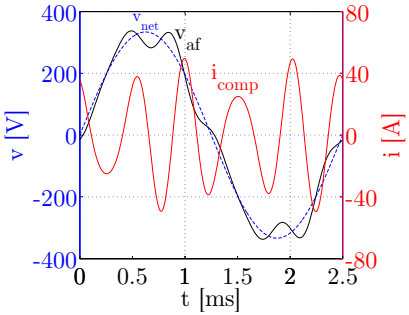


Figure 5.2: Compensation current i_{comp} and voltage v_{af} at the active filter output (L_f=80 µH).

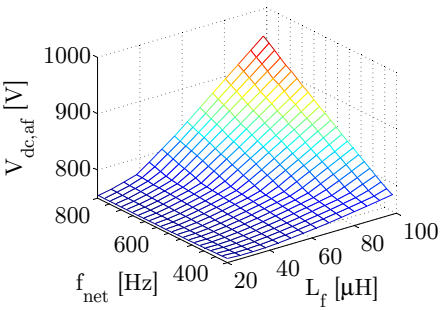


Figure 5.3: Required voltage at active filter DC-link dependent on f_{net} and L_f.

for $\frac{2}{3}$rd of the time due to the rectifier. The necessary voltage, which has to be generated by the APF, is

$$v_{af}(t) = v_{net}(t) + v_{comp}(t) \tag{5.4}$$

with

$$v_{net}(t) = \hat{V}_{net} sin(\omega_{net} t) \tag{5.5}$$

and

$$v_{comp}(t) = \frac{d}{dt} i_{comp}(t) L_f \tag{5.6}$$

(fig. 5.2). $\hat{V}_{net}$ is the amplitude of the supply voltage before the source inductance L_{net}. The required voltage $V_{dc,af}$ at the active filter DC-link is

$$V_{dc,af} = \frac{2\hat{v}_{af}}{\hat{m}}(1 + k_{dc}), \tag{5.7}$$

where $\hat{m}$ is the desired maximum modulation and k_1 a design margin. To enable the use of semiconductor devices with 1200 V rating and taking into account the decreased voltage blocking capability at low temperatures, the voltage $V_{dc,af}$ should not exceed 900 V. Furthermore, the lower this voltage is, the lower the CM-voltages and corresponding CM-currents become. Fig. 5.3 depicts $V_{dc,af}$ as a function of L_f and f_{net} with $\hat{m}$=95% and margin $k_1 = 10\%$. To achieve the 900 V requirement, L_f is set to 80 µH for the further design process.

The APF injects harmonics into the main supply, which leads to an AC power flow delivered by the APF DC-link. The resulting voltage ripple at the DC-link has a frequency of $6f_{net}$, the amplitude is dependent on the

size of $C_{dc,af}$. The APF AC power is described by

$$\begin{aligned} p_{af}(t) = v_a(t)i_{comp,a}(t) + v_b(t)i_{comp,b}(t) + v_c(t)i_{comp,c}(t) \\ = \hat{p}_{af} sin(6\omega_{net}t) \end{aligned} \tag{5.8}$$

and depicted in fig. 5.4. $\hat{p}_{af}$ can be simplified to

$$\hat{p}_{af}(360\ Hz) \approx V_{net}\left(2.028\hat{I}_5 + 1.086\hat{I}_7\right) \tag{5.9}$$

as described in chapter A.1.2. The highest value of $\hat{p}_{af}$ appears for $f_{net} = 360Hz$ and $V_{net} = 236V$. That is why this formula is only valid for this operation point.

The DC-link voltage ripple caused by p_{af} can be limited purely by the size of DC-link capacitance. The necessary capacitance is

$$C_{dc,af} = \frac{\hat{p}_{af}}{6\pi f_{net} V_{dc,af}\left(\frac{k_2}{4} + k_2\right)} \tag{5.10}$$

with k_2 as peak-to-peak voltage ripple related to $V_{\mathrm{dc,af}}$ and peak power delivered by APF DC-link $\hat{p}_{af}$.

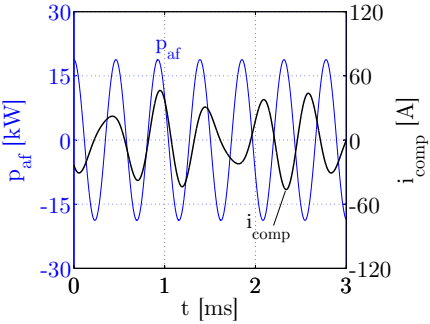


Figure 5.4: Compensation current and AC power flow, which has to be delivered by APF DC-link.

5.3 Design of DC-link chokes

The active filter acts as a current source and hence influences the main DC-link. The voltage ripple is increased, which could cause torque fluctuations in the motor. The biggest component of the DC-link ripple is the 6^{th} harmonic. The allowed value is 17.8 V_{pp} (tab. 2.4). To fulfil this requirement, additional inductors L_{dc} are necessary. The required value is strongly dependent on the DC-link capacitance as depicted in Fig. 5.5. Choosing a bigger capacitance decreases the necessary value for L_{dc}, but increases the peak compensation current $\hat{I}_{comp}$. Due to the prohibition of electrolytic capacitors for aerospace applications, only foil capacitors are available, which are quite bulky with several hundred µF. Therefore, the value for C_{dc} is chosen with respect to the available volume.

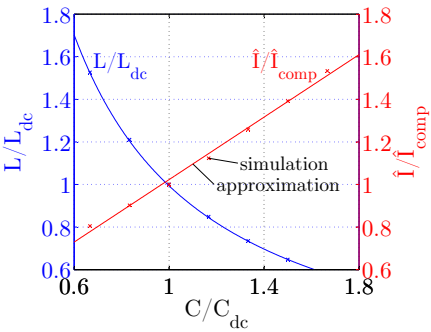


Figure 5.5: L and $\hat{I}$ versus DC-link capacitance for $v_{pp} = 17.8V$. All values are normalized to the chosen design with L_{dc} and C_{dc}.

The results in Fig. 5.5 are derived by simulations. The voltage ripple is kept constant at 17.8 V_{pp}. The required inductance can be approximated by potential function

$$L_{dc,r} = 18575 C_{dc}^{-1,047} \frac{\mu H}{\mu F} \tag{5.11}$$

and the peak compensation current by linear function

$$\hat{I}_{comp} = 0{,}1153 C_{dc} \frac{A}{\mu F} + 14{,}605 A. \tag{5.12}$$

In the following, the design of the DC-link choke is explained. The input parameters are the required inductance ($L_{dc,r}$) and the peak DC current ($\hat{I}_{dc}$). The parameters core material, core type, core size, wire cross section, number of windings and air gap have to be determined. SiFe is chosen as core material, since the main component is a DC current. There are no high frequency currents, which would induce high iron power loss in SiFe. Due to the small number of windings, two stacked 60 mm SiFe ring cores are used for the choke. Higher number of windings require a cut C-core with bobbins to simplify the choke production. The wire cross section is

defined via the current density, which may be ∼4 A/mm^2 without any cooling and ∼8 A/mm^2 with potting and liquid cooling. These figures are experience values. The required number of windings is calculated through

$$n_r = \frac{L_{dc,r}\hat{I}_{dc}}{B_{sat}A_c} \tag{5.13}$$

with saturation flux density B_{sat} (1.6 T in SiFe) and core cross section A_c (fig. 5.6). After rounding the required n_r to an integer, the required value of inductive constant $A_{L,r}$ can be derived from

$$A_{L,r} = \frac{L_{dc,r}}{n_r^2}. \tag{5.14}$$

The required effective relative permeability is

$$\mu_{eff,r} = \frac{2\pi A_{L,r}}{ln\left(\frac{D_o}{D_i}\right)\mu_0 h_c} \tag{5.15}$$

[107] with magnetic constant μ_0, outer core diameter D_o, inner core diameter D_i and core height h_c (fig. 5.6).

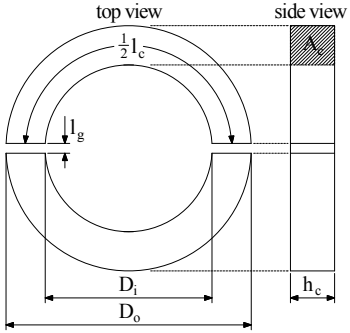


Figure 5.6: Dimensions of cut magnetic ring core with two air gaps. The core consists of wound SiFe tape with 0.1 mm thickness.

The resulting required air gap is

$$l_{g,r} = \frac{l_c(\mu_{eff,r} - \mu_c)}{2\mu_c(1 - \mu_{eff,r})} \tag{5.16}$$

with effective magnetic path length l_c and relative permeability μ_c of the magnetic material. One half of the magnetic ring core has the path length $\frac{1}{2}l_c$ (Fig. 5.6). The total magnetic path length is then l_c considering two

half cores. In this example two air gaps are present. This is taken into account by the factor 2 in the denominator. The stray or fringing flux in the air gap results in a higher inductance and lower saturation than calculated. This effect is taken into account by the fringing flux factor F_r [108]. The calculated air gap must be corrected applying the fringing flux factor:

$$l_{g,corr} = \frac{l_c(\frac{\mu_{eff,r}}{F_r^2} - \mu_c)}{2\mu_c(1 - \frac{\mu_{eff,r}}{F_r^2})}. \tag{5.17}$$

with

$$F_r = 1 + \frac{l_{g,corr}}{\sqrt{A_c}} ln\Big(\frac{2D_i}{l_{g,corr}}\Big). \tag{5.18}$$

Due to the two air gaps, the fringing flux factor is squared. The conjunction of eq. 5.17 and eq. 5.18 is an implicit function and hence must be solved by manual iteration or numerical means. The resulting air gap $l_{g,corr}$ is the physical necessary air gap. The air gap is established typically by FR4 or polyester materials such as hostaphan. Since the thicknesses are only available in discrete steps, the real possible air gap will be different. With the chosen feasible air gap l_g, the effective relative permeability can be derived from

$$\mu_{eff} = \frac{2l_g + l_c}{\frac{l_c}{\mu_c} + 2l_g}. \tag{5.19}$$

The resulting A_L-value is

$$A_L = F^2 \frac{\mu_0 \mu_{eff} h_c}{2\pi} ln\Big(\frac{D_a}{D_i}\Big) \tag{5.20}$$

[107] with

$$F = 1 + \frac{l_g}{\sqrt{A_c}} ln\Big(\frac{2D_i}{l_g}\Big). \tag{5.21}$$

The necessary number of windings is

$$n_r = \sqrt{\frac{L_{dc,r}}{A_L}}. \tag{5.22}$$

After rounding the calculated n_r to an integer, the resulting inductance can be calculated through

$$L_{dc} = A_L n^2. \tag{5.23}$$

with chosen integer number of windings n. The peak flux density $\hat{B}$ in this

case must be lower than 1.6 T to avoid saturation:

$$\hat{B} = \frac{L_{dc}\hat{I}_{dc}}{nA_c} \tag{5.24}$$

The BH-curve is derived from the measurement of voltage and current at a test coil with SiFe core (fig. 5.7). Due to the presence of an air gap, the hysteresis of the BH-curve is negligible. The resulting BH-curve after removing the hysteresis is depicted in fig. 5.7. The differential relative material permeability is derived from the simplified BH-curve (fig. 5.8). The characteristic is strongly dependent on the flux density. With air gap, the resulting effective relative permeability (eq. 5.19, fig. 5.8) is nearly constant up to 1.4 T, which results in a nearly constant inductance in this range.

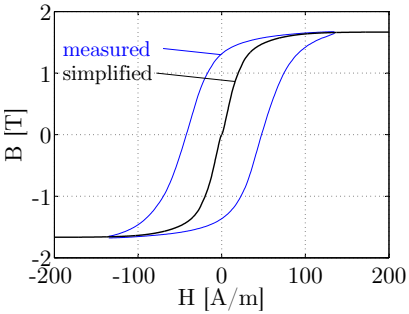


Figure 5.7: Measured and simplified BH-curve of cut SiFe C-core without air gap.

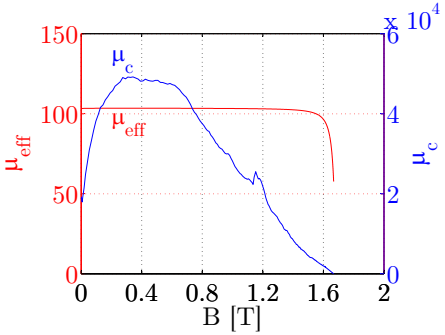


Figure 5.8: Relative permeability of ungapped SiFe core (μ_c) and effective relative permeability with air gap (μ_{eff}).

The final characteristic of the L_{dc} prototype is depicted in fig. 5.9. A system simulation with APF, rectifier and load, taking into account the measured inductance characteristic, shows that this design is compliant with the DC-link voltage ripple requirement, i.e. the DC-link voltage ripple remains below 17.8 V_{pp}. This simulation is performed at worst case condition with lowest supply frequency (360 Hz) and highest input phase voltage ($236V_{RMS}$).

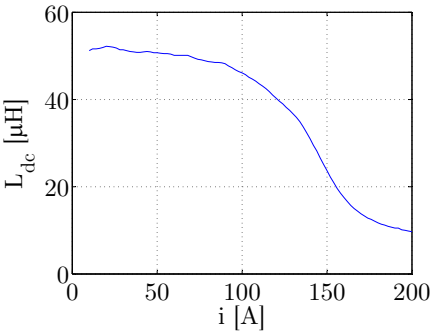


Figure 5.9: Inductance vs. current of L_{dc} prototype.

5.4 Design of inverter stage

5.4.1 Electrical characterization of semiconductor switches

For the active power filter, two power modules in the SP3-case are characterized and evaluated (see also [109] and [110]):

- 1200V / 100A non-punch-through-IGBT (NPT-IGBT) with ultrafast free-wheeling diodes ([111])
- 1700V / 40A SiC-MOSFET with SiC free-wheeling diodes ([112])

The 1200 V modules are used in the laboratory setup only, since the SiC modules were not available at the beginning. As already discussed, the 1200 V modules do not offer enough margin against cosmic radiation. For the series production of the APF, only the 1700 V SiC-MOSFET is a possible power switch. The SiC power module is a customized part and therefore explained in detail in this section.

One SiC power module (fig. 5.10) contains a half bridge. The MOSFET consists of two dies in parallel, since one die is rated for 20 A only. In principle, the diodes D_1 and D_2 are not necessary due to the reverse conduction capability of the MOSFET. However, the integration of an additional series diode D_1 and free-wheeling diode D_2 was recommended by the MOSFET manufacturer to avoid a thermal overload of the MOSFET. The used MOSFETs were samples for research purpose only and were not released for series products. The diode D_1 prevents a current flow through the MOSFET during the free-wheeling phase. Without D_1,

the free-wheeling currents would flow through MOSFET and D_2 simultaneously. The current distribution between MOSFET and diode is complex due to the dependency on current and junction temperature. The calculation of this current sharing can be calculated only by means of simulation.

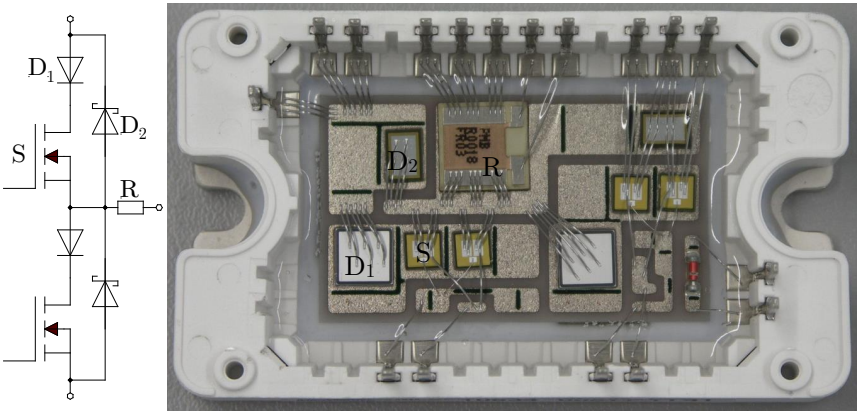


Figure 5.10: Schematic and structure of SP3 module with series diode (D_1), two MOSFET dies in parallel (S), free wheeling diode (D_2) and shunt (R) for current measurement.

The characterization of power modules is performed in a special test setup (fig. 5.11) with low inductive DC-link, 1 GHz oscilloscope, 2 GHz coaxial shunt for current measurement, 200 MHz differential voltage probe and LabView for automation and calculation of E_{on}, E_{off} and E_{rr}. During switching measurements, the top switch is deactivated and the bottom switch is clocked with a double pulse. The length of the double pulse depends on required test current and size of air choke L_a.

The oscilloscope is supplied via an insulating transformer to avoid a ground loop with the earthed test setup. The conduction characteristic is measured with curve tracer 371A from Sony/Tektronix and a heating plate for the 125 °C measurements. The results for junction temperatures of 25 °C and 125 °C are compared with the NPT-IGBT (fig. 5.12). Up to 60 A, the MOSFET offers lower conduction voltages. Since this active filter application generates AC currents in the the range from -60 to 60 A, the conduction losses of the inverter are lower, too (tab. 5.3).
The use of a Rogowski coil for current measurements during characterization of IGBTs is quite common. However, the characterization of these SiC switches reveals the limit of the used Rogowski coil. Compared to a 2 GHz coaxial shunt, the Rogowski coil has a delay of about 28 ns and

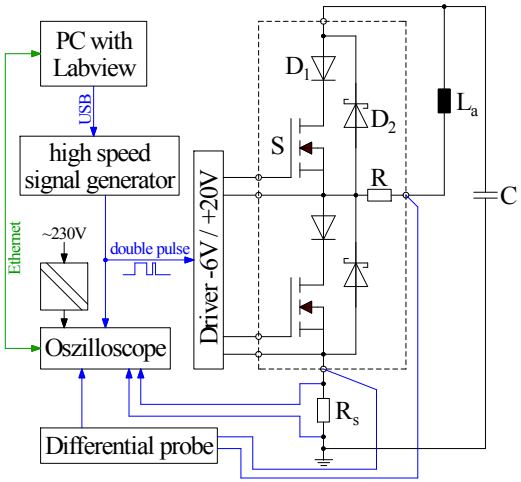


Figure 5.11: Laboratory test setup for semiconductor characterization.

cannot follow the steep current characteristic (fig. 5.13). That is why all measurements are performed with the coaxial shunt.
The gate resistor R_{Gon} is set to 5 Ω for all further measurements. The E_{on} for different currents and temperatures is displayed in fig. 5.19. At 125 °C the turn-on energy is lower than at 25 °C.

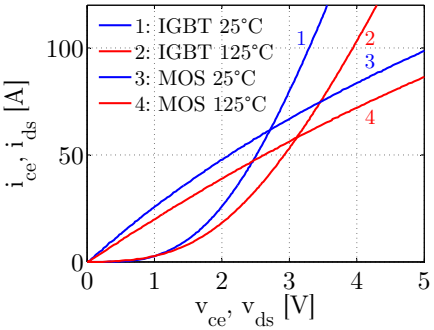


Figure 5.12: Conduction characteristics of SiC-MOSFET and NPT-IGBT for 25 °C and 125 °C junction temperatures.

The design of gate resistor R_{Goff} is not as straightforward as for R_{Gon}. Due to high voltage overshoot of v_{ds} with subsequent oscillation, the choice of appropriate gate resistor is more important. Current i_{ds} and voltage v_{ds} for different values of R_{Goff} are shown in fig. 5.15 and fig. 5.16. The switching energy E_{off}, dv/dt and di/dt dependent on R_{Goff} are summarized in fig.

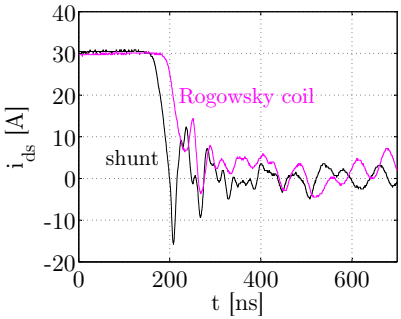


Figure 5.13: Comparison of measured currents with 20 MHz Rogowski coil and 2 GHz 50 mΩ coaxial shunt.

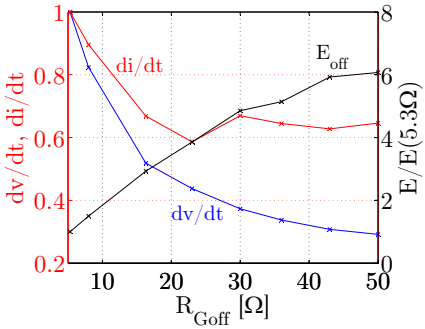


Figure 5.14: dv/dt, di/dt and E_{off} vs. R_{Goff} (normalized to 5 Ω).

5.14. Until R_{Goff}=16 Ω, di/dt decreases to about 65 % of the value at 5 Ω. A further increase of R_{Goff} has hardly any additional influence. Only the switching-off delay increases (fig. 5.15), which results in higher values for E_{off}. Since the voltage overshoot is caused by di/dt, a higher resistance than 16 Ω does not achieve significant improvements. That is why R_{Goff} is fixed to 16 Ω for all further measurements. Fig. 5.17 shows v_{ds} and i_{ds} during switching-on. The current overshoot is caused by the intrinsic capacitances of the SiC diode. Fig. 5.18 depicts v_{ds} and i_{ds}. The voltage overshoot is 100 V and the ringing has a frequency of about 30 MHz.

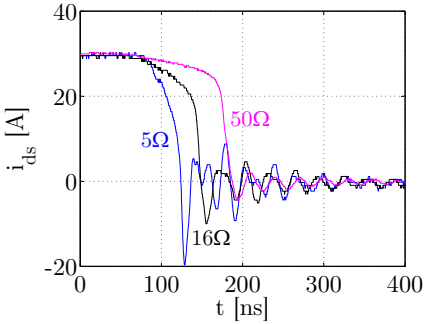


Figure 5.15: i_{ds} during switching-off for different gate resistor R_{Goff}.

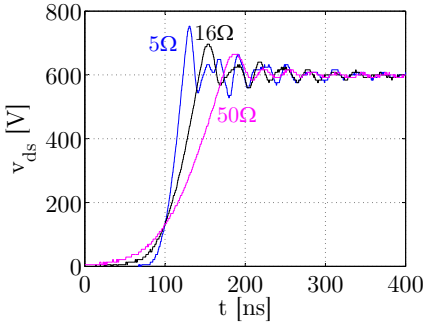


Figure 5.16: v_{ds} during switching-off for different gate resistor R_{Goff}.

Both E_{on} and E_{off} decrease with higher junction temperature (fig. 5.19, fig. 5.20) in contrast to IGBTs. However, this behaviour seems not to be equal for all SiC-MOSFETS. The power module BSM120D12P2C005 from

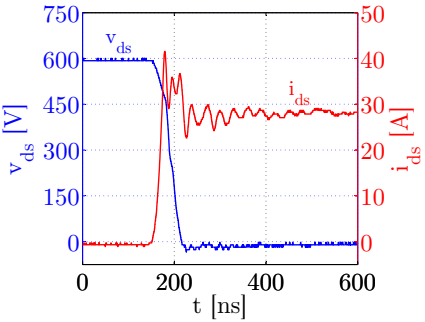


Figure 5.17: Switching-on characteristic @ 600 V / 30 A (R_{Gon}= 5 Ω).

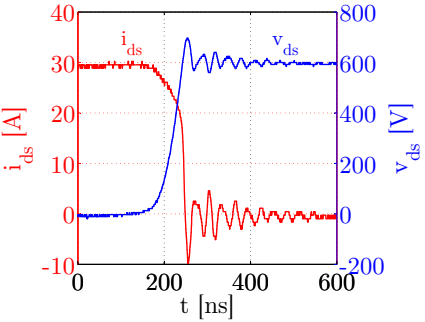


Figure 5.18: Switching-off characteristic @ 600 V / 30 A (R_{Goff}= 16 Ω).

Rohm shows an increasing E_{off} and a decreasing E_{on} with higher junction temperature [113].

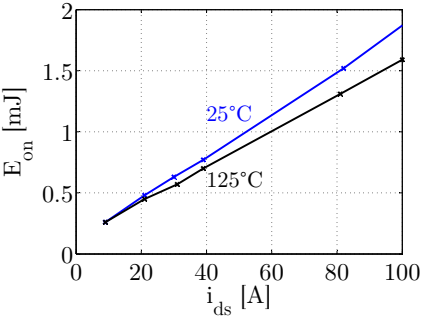


Figure 5.19: E_{on} vs. current for 25 °C and 125 °C (R_{Gon}=5 Ω)

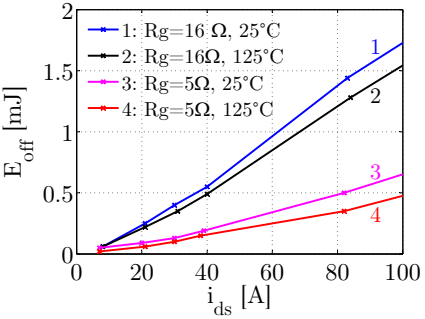


Figure 5.20: E_{off} vs. current for 25 °C and 125 °C (R_{Goff}=5 Ω and 16 Ω)

The conduction characteristics of the free-wheeling diodes at 25 and 125 °C are depicted in fig. 5.21. As expected, the SiC-diode shows a significantly higher forward voltage drop. In contrast to the standard diode, the SiC-diode exhibits higher conduction losses at 125 °C, which simplifies the paralleling of several SiC-diodes.
The diode switching losses in fig. 5.22 are caused by the reverse recovery charge (standard diode) and the intrinsic capacitance (SiC-diode). Due to the higher voltage blocking capability of SiC material, the resulting chips are thinner and therefore have a higher intrinsic capacitance. The E_{rr} of the SiC-diode changes linearly with the applied current. The E_{rr} vs. current characteristic of the ultra-fast Si-diode can be approximated by an

exponential:

$$E_{rr1}(i) = E_{rr1,end}\left(1 - e^{-\frac{i}{i_{rr1}}}\right) \tag{5.25}$$

with $E_{rr1,end} = 3.72mJ$ and $i_{rr1} = 59.0A$. To simplify the loss calculation, the e-function $\mathrm{E_{rr1}(i)}$ is approximated by a linear function $\mathrm{E_{rr2}(i)}$, which is valid up to the maximum compensation current of $\hat{I}_{comp}$:

$$E_{rr2}(i) = 2E_{rr1,end}\frac{\hat{I}_{comp} + i_{rr1}\left(e^{-\frac{\hat{I}_{comp}}{i_{rr1}}} - 1\right)}{\hat{I}^2_{comp}} \cdot i \tag{5.26}$$

with $\hat{I}_{comp} = 50A$. The slope of $\mathrm{E_{rr2}}$ is derived using the following approach:

$$\int_0^{\hat{I}_{comp}} \left[E_{rr1}(i) - E_{rr2}(i)\right] di = 0 \tag{5.27}$$

At the maximum compensation current of $\hat{I}_{comp}$, E_{rr2} has a value of

$$E_{rr2}(50A) = 2E_{rr1,end}\left(1 + \frac{i_{rr1}}{\hat{I}_{comp}}\left(e^{-\frac{\hat{I}_{comp}}{i_{rr1}}} - 1\right)\right) \approx 2.42mJ. \tag{5.28}$$

This parameter is used for the power loss calculation in chapter 5.4.3. Tab. A.2 and tab. A.2 compare all parameters derived from the datasheet and the characterization measurements. For the loss calculation, the worst case values are used. The final parameters, used for the power loss calculation, are summarized in tab. 5.1. Since the E_{rr} of the SiC-diode changes linear with the current, an approximation is not necessary and thus the parameters E_{rr2}, $I_{test,Err2}$ and $V_{test,Err2}$ are identical to E_{rr}, $I_{test,Err}$ and $V_{test,Err}$.

The evaluation of SiC-MOSFET with respect to electromagnetic compatibility (EMC) is done via measurement of common-mode (CM) voltages (fig. 5.23) at the output of the inverter and CM currents (fig. 5.24) at the DC-link input. These results are compared with the NPT-IGBT to see the impact of SiC switching speed. The test is done with standard sinusoidal PWM (90 % modulation), switching frequency of 60 kHz and DC-link voltage of 540 V. EMC filters are not present. Up to frequencies of 1 MHz, the CM voltages of MOSFET and IGBT are nearly identical. At frequencies above 1 MHz, the higher switching speed of SiC causes levels,

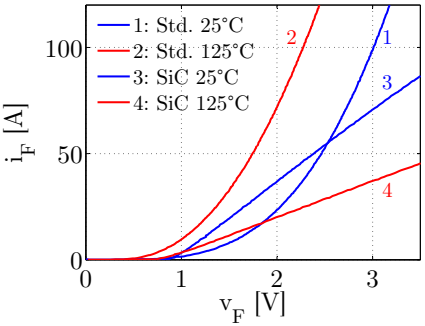


Figure 5.21: Conduction characteristic of standard and SiC diode for 25 and 125 °C.

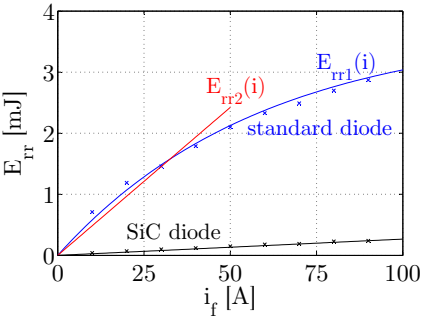


Figure 5.22: Switching losses of standard and SiC diode for 125 °C.

Parameter	IGBT module	MOSFET module
E_{on} [mJ]	12,00	0,63
E_{off} [mJ]	5,00	0,41
V_{test} [V]	600	600
I_{test} [A]	100	30
E_{rr} [mJ]	3,04	0,28
$V_{test,Err}$ [V]	600	600
$I_{test,Err}$ [A]	100	100
$E_{rr1,end}$ [mJ]	3,72	-
τ_{rr} [A]	59,0	-
E_{rr2} [mJ]	2,42	0,28
$V_{test,Err2}$ [V]	600	600
$I_{test,Err2}$ [A]	50	100
V_{ce0} [V]	2,18	-
r_{ce}, R_{ds} [mΩ]	20,9	61,0
V_{f0} [V]	1,3	0,8
r_f [mΩ]	11,7	75,0

Table 5.1: Electrical characterization results at T_J=125 °C.

which are up to 20 dBµV higher. The resulting CM current is higher, too. The radiated emission was not measured, since the radiation is strongly dependent on the final mechanical structure, shielding method and output cable lengths. If the cable length is known, an estimation using the output

CM current can be performed as described in [114].

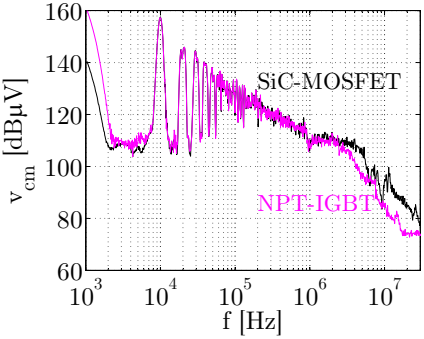


Figure 5.23: Comparison of CM voltage spectrum at the output of IGBT and SiC inverters.

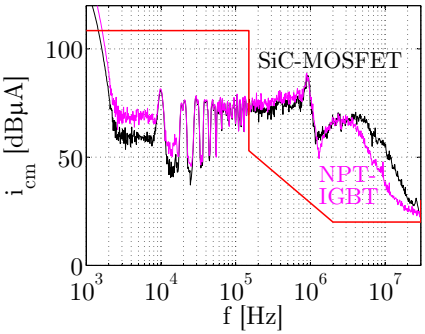


Figure 5.24: Comparison of CM current spectrum at the DC-link input.

5.4.2 Thermal characterization

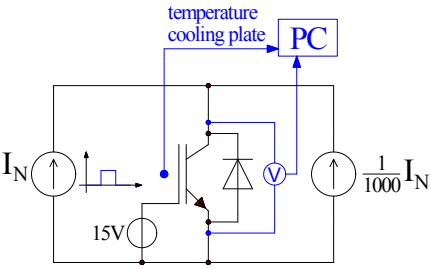


Figure 5.25: Test setup for deriving of thermal impedance Z_{th}.

The $V_{CE}(T)$-method is used to derive the thermal impedance between cooling plate and semiconductor chip. This method is described in detail in [115]. Since the diffusion voltage of pn-junction and Schottky barrier are dependent on the temperature, the chip itself can be used as temperature sensor. Before the measurement, the "sensor" must be calibrated, i.e. the forward voltage drop at a defined test current vs. temperature must be measured. The calibration results for the NPT-IGBT and the SiC-diode are depicted in fig. 5.26 and are approximated with a linear function. The test setup for the thermal impedance is described in fig. 5.25. The chip is heated to 150 °C by a pulse with nominal current. After the pulse, the forward voltage of the IGBT or diode is measured and analyzed by a computer. During the measurement a test current of $\frac{1}{1000} I_N$ is applied (I_N is the nominal current of the power module).

The measured thermal impedances are displayed in fig. 5.27 and approximated via three-stage foster model. The foster model parameters (tab. 5.2) are extracted with the solver function in Mathcad. Only the NPT-IGBT and SiC-diode are measured. The Si-diode and SiC-MOSFET parameters are scaled linearly according to the area difference. Hence, the resulting thermal resistors of the Si-diode are higher and the thermal capacitors are lower due to the smaller chip area. The SiC-MOSFET chip area is bigger and therefore the thermal resistors are lower and the thermal capacitors are higher compared to the SiC-diode.

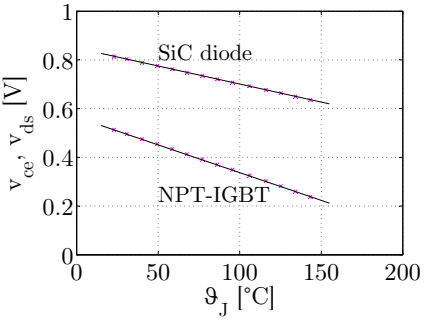


Figure 5.26: Forward voltage drop at $\frac{1}{1000} I_N$ vs. junction temperature.

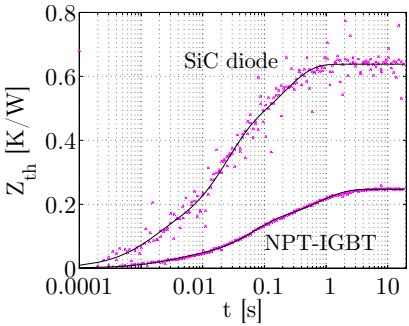


Figure 5.27: Measured Z_{th} curves with approximation.

	IGBT module	MOSFET module
Thermal resistance		
$R_{thJCP,S}$ [K/W]	0,24	0,52
$R_{thJCP,D}$ [K/W]	0,59	0,64
Thermal impedance		
R_{S1} [K/W]	0,03	0,09
C_{S1} [J/K]	0,15	0,01
R_{S2} [K/W]	0,11	0,25
C_{S2} [J/K]	0,60	0,09
R_{S3} [K/W]	0,10	0,18
C_{S3} [J/K]	8,42	1,21
R_{D1} [K/W]	0,08	0,11
C_{D1} [J/K]	0,06	0,01
R_{D2} [K/W]	0,27	0,31
C_{D2} [J/K]	0,25	0,07
R_{D3} [K/W]	0,24	0,22
C_{D3} [J/K]	3,47	0,99

Table 5.2: Thermal characterization results measured at T_J=150 °C.

5.4.3 Losses and temperatures

For the calculation of semiconductor losses, the compensation current is defined as

$$i_{comp}(i) = \hat{I}_5 sin(5\omega_{net}t) + \hat{I}_7 sin(7\omega_{net}t) \tag{5.29}$$

with $\omega_{net} = 2\pi f_{net}$. The calculation is performed over one period T_p of the supply frequency. T_p is calculated using

$$T_p = \frac{1}{f_{net}}. \tag{5.30}$$

The RMS-value of i_{comp} is

$$I_{comp} = \sqrt{\frac{1}{T_p}\int_0^{T_p} i_{comp}^2(t)dt} \tag{5.31}$$

and the average absolute value is

$$\bar{I}_{comp} = \frac{1}{T_p}\int_0^{T_p} |i_{comp}(t)|dt. \tag{5.32}$$

With the given ripple filter inductance and the supply voltage, the APF output voltage v_{af} can be calculated (fig. 5.28). In motor drive applications, the mean and effective currents through diodes and switches depend on modulation index m and $cos\varphi$. The currents through the switches increase with higher m and higher $cos\varphi$, the diode currents behave inversely. Considering a compensation current without fundamental component and neglecting the PWM dead time, the current distribution in the active power filter application is independent of m and $cos\varphi$. The compensation current has positive and negative values during both half waves of the APF output voltage v_{af}. A higher m results in a

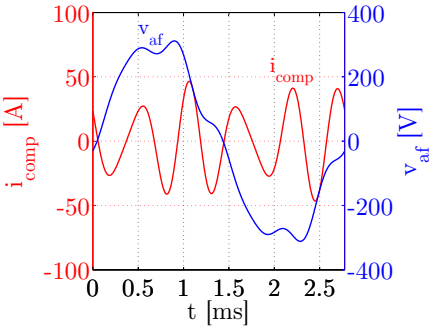


Figure 5.28: Compensation current and APF output voltage used for the calculation of semiconductor losses.

higher conduction current during the first half wave of v_{af} (for the switch), but lowers the conduction current in the second. On average, the conduction current does not change. The current through the diodes behaves inversely. With average modulation index $\bar{m} = \frac{1}{2}$, the average conduction current through switches and diodes can be calculated through

$$\bar{I}_{cond} = \frac{1}{2}\bar{I}_{comp}\bar{m} = \frac{1}{4}\bar{I}_{comp}. \tag{5.33}$$

The RMS current through switch and diode is derived by the same approach:

$$I_{cond} = \sqrt{\frac{1}{2}I_{comp}^2\bar{m}} = \frac{1}{2}I_{comp} \tag{5.34}$$

The conduction and switching power loss are dependent on the junction temperature. Since only the values at $T_J = 125°C$ are available, the following formulas are valid for 125°C only. The conduction power loss is calculated using the common approximation with forward voltage and differential resistance. The formula for the diode is

$$P_{cond} = \frac{1}{T_p}\int_0^{T_p} v_f(t)i_f(t)dt \approx \bar{I}_{cond}V_{f0} + I_{cond}^2 r_f. \tag{5.35}$$

This formula is used for the IGBT conduction loss, too. The parameters V_{f0} and r_f are replaced by V_{ce0} and r_{ce} in this case. For the MOSFET conduction loss, only parameter R_{ds} is necessary.
A simplified approach to calculate the semiconductor switching losses is the assumption of linear dependency between DC-link voltage and the energies E_{on}, E_{off} and E_{rr}. The E_{on} and E_{off} dependencies vs. current are linear, too, as the measurements in fig. 5.19 and fig. 5.20 show. The switching losses of IGBT and MOSFET are then

$$P_{sw,S} = f_{sw}\frac{1}{2}\frac{\bar{I}_{comp}}{I_{test}}\frac{V_{dc,af}}{V_{test}}\Big[E_{on} + E_{off}\Big] \tag{5.36}$$

with switching frequency f_{sw}, DC-link voltage $V_{dc,af}$, test current at characterization I_{test} and test voltage at characterization V_{test}. The factor $\frac{1}{2}$ is due to the fact that the switch conducts only during positive or negative compensation current. The dependency of E_{rr} vs. current is linear for the SiC-diode and approximated by the linear function E_{rr2} for the standard

diode (fig. 5.22). The diode losses are then

$$P_{sw,D} = f_{sw} \frac{1}{2} \frac{\bar{I}_{comp}}{I_{test,Err2}} \frac{V_{dc,af}}{V_{test,Err2}} E_{rr2} \tag{5.37}$$

with test current at characterization $I_{test,Err2}$ and test voltage at characterization $V_{test,Err2}$. The factor $\frac{1}{2}$ is due to the fact that one diode conducts only during positive or negative compensation current.

All relevant parameters can be found in tab. 5.1. The steady state results, normalized to the IGBT's switching losses, are summarized in tab. 5.3. The switching loss reduces by 80 % using the SiC-MOSFET. The conduction power loss does not change significantly.

	IGBT module	**MOSFET module**	**rectifier module**
$P_{sw,S}$	1,00	0,20	n.A.
$P_{cond,S}$	0,09	0,06	n.A.
$P_{sw,D}$	0,29	0,02	n.A.
$P_{cond,D}$	0,05	0,10	0,29
$\mathbf{P_{sum}}$	**1,43**	**0,38**	**0,29**

Table 5.3: Normalized power losses of power semiconductors (T_J=125 °C).

The transient power loss in the IGBT chip is depicted in fig. 5.30 and the corresponding spectrum in fig. 5.29. With the damping characteristic of the thermal impedance Z_{th} (fig. 5.29), the transient junction temperature can be derived taking into account 89 °C cooling plate surface temperature (fig. 5.30). The cooling plate surface temperature is described in chapter 2.6. The mean junction temperatures have values of 134 °C (NPT-IGBT) and 112 °C (SiC-MOSFET). These values are not critical, since the IGBT is rated for a junction temperature of maximum 150 °C ([111]) and the SiC-MOSFET for 175 °C ([116]). The total power loss of the SiC-MOSFET is 75% lower compared to the IGBT (tab. 5.3). However, due to the significantly higher thermal impedance of the SiC-MOSFET chips (tab. 5.2), the junction temperatures show a quite low difference of 22 °C only.

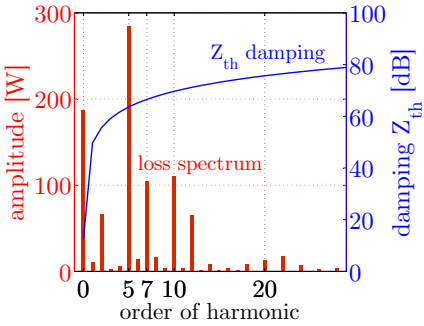


Figure 5.29: Spectrum of chip losses in IGBT and damping of IGBT Z_{th}.

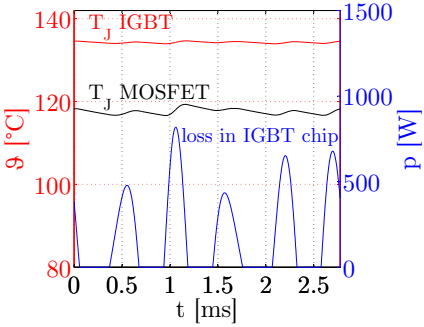


Figure 5.30: Losses of IGBT chip and junction temperatures of IGBT and MOSFET.

5.5 EMC and filter design

5.5.1 Differential mode filter

The ripple filter at the output of the APF dampens the noise generated by the switching of the active filter. For the filter design, a spectrum of v_{comp} is necessary. This can be derived by generating the switching vectors and the resulting voltages with a Matlab m-file. The result is depicted in fig. 5.31 (time domain) and fig. 5.32 (frequency domain).

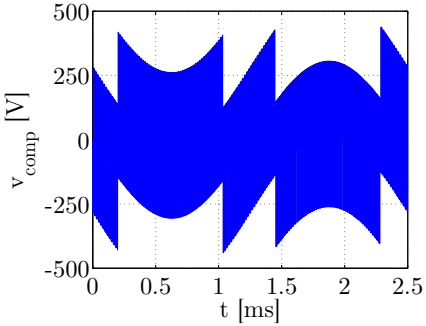


Figure 5.31: Switched voltage generated by the APF inverter.

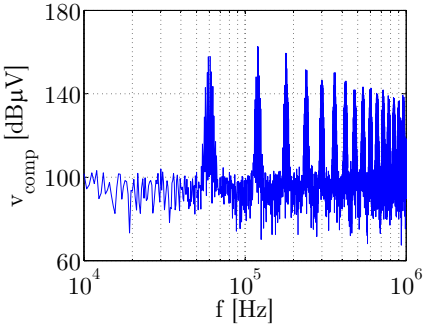


Figure 5.32: Spectrum of switched voltage in fig. 5.31.

The ripple current caused by the duplex inverter with a switching frequency of 10 kHz is not considered. Inductor L_{dc} and DC-link capacitor C_{dc} form a low-pass filter with a resonant frequency of 1370 Hz. Furthermore, the duplex topology with 180° phase shift between the two PWM

carriers results in significantly lower current ripple in the DC-link.

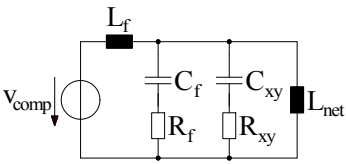


Figure 5.33: Ripple filter with one LC-stage.

The simplest filter topology consists of only one LC-stage and source inductance L_{net}. The corresponding single-phase model, derived from the overall schematic in fig. 5.1, is shown in fig. 5.33. At frequencies above 150 kHz, the source impedance is defined by a LISN as described in chapter 3.3. DC-link inductor L_{dc} and capacitor C_{dc} are not taken into account, since this path is nonlinearly connected to the rectifier. The main input filter has further differential and common mode capacitances, too. This is taken into account by capacitance C_{xy}. The two common-mode chokes with their stray inductances are not considered in the following approach, since the values are negligibly small compared to the ripple filter inductances.
The ripple filter influence is depicted in fig. 5.34. The damping characteristic has a minimum at resonant frequency f_r (damping resistors are not taken into account) with

$$f_r = \frac{1}{2\pi\sqrt{\frac{L_f L_{net}}{L_f + L_{net}}\left(C_f + C_{xy}\right)}} \tag{5.38}$$

with $C_{xy} = C_x + C_y$. Due to this ripple filter, the phase current in time domain shows a ringing with frequency f_{ring} (fig. 5.35), which is defined by

$$f_{ring} = \frac{1}{2\pi\sqrt{L_{net}\left(C_f + C_{xy}\right)}}. \tag{5.39}$$

Both f_r and f_{ring} are only dependent on capacitance C_f, since L_f and L_{net} are already defined. f_{ring} is chosen as 25 kHz, which is low enough to achieve a considerable filter damping at the switching frequency and high enough to avoid interaction with the low frequency harmonics. The necessary value of C_f is calculated through

$$C_f = \frac{1}{\left(2\pi f_{ring}\right)^2 L_{net}} - C_{xy}. \tag{5.40}$$

The consequence of the ringing is a non-compliance of harmonics 29, 31, 35 and 37 in the corresponding phase current spectrum (fig. 5.36). This effect can be eliminated by a higher damping resistor of 7 Ω instead of 0.5 Ω, which results in 76 % higher loss and significantly lower damping

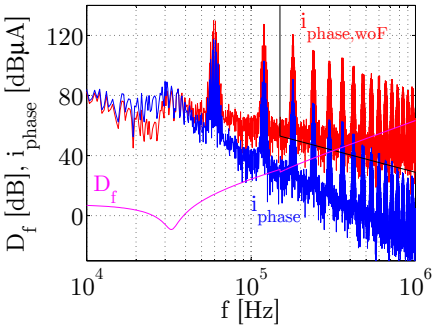


Figure 5.34: Ripple filter damping and spectrum of phase current with and without ripple filter according to fig. 5.33.

capability at higher frequencies. This result is derived from a simulation with a filter capacitance C_f according to eq. 5.40.

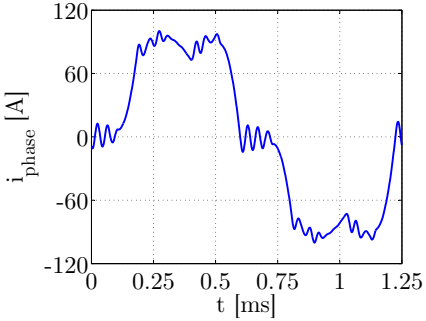


Figure 5.35: Phase current with ripple filter according to fig. 5.33 (APF deactivated).

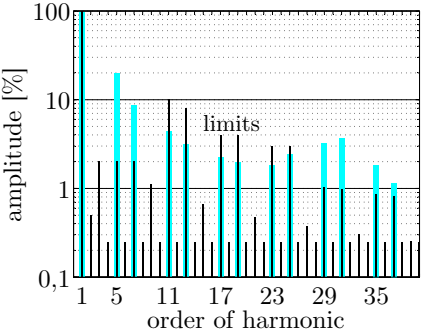


Figure 5.36: Spectrum of current in fig. 5.35.

A higher damping resistor of 7 Ω is not the preferred solution. Alternatively, a damping resistor parallel to C_f could be considered. However, the fundamental voltage across C_f is the supply voltage of nominal 230 V. To achieve similar losses as calculated in fig. 5.34, a resistance of 2.1 kΩ would be necessary. At the ringing frequency of 25 kHz, the impedance of C_f is about 10 Ω and therefore a damping resistance of 2.1 kΩ will not have any effect.

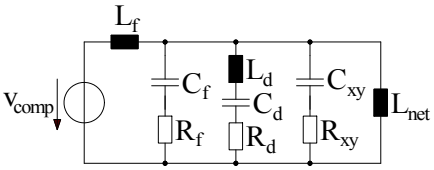


Figure 5.37: Ripple filter model with parallel damping.

To lower the damping resistor, an LC-stage is integrated parallel to C_f and serially to R_d with a resonant frequency of f_{ring} (fig. 5.37). The low frequency high voltage amplitude is filtered out by C_d and the resonant with L_d enables maximum damping for the resistor at f_{ring}. Furthermore, L_d prevents a current flow through R_d at higher frequencies, which would lead to additional losses. At the highest supply frequency of 800 Hz, the impedance of C_d shall be 100 times above R_d as first assumption. This is expressed by

$$C_d = \frac{1}{100 R_d \cdot 2\pi 800 Hz}. \tag{5.41}$$

L_d is designed with respect to the desired resonant frequency of f_{ring}:

$$L_d = \frac{1}{(2\pi f_{ring})^2 C_d} \tag{5.42}$$

The simulation results in fig. 5.38 and fig. 5.39 show that the ringing amplitude is lower and harmonics between 29$^{\text{th}}$ and 37$^{\text{th}}$ are compliant. The damping characteristic in fig. 5.40 does not show big differences to fig. 5.34, but the total damping losses are reduced by 42 % compared to the model in fig. 5.33 with 0.5 Ω.

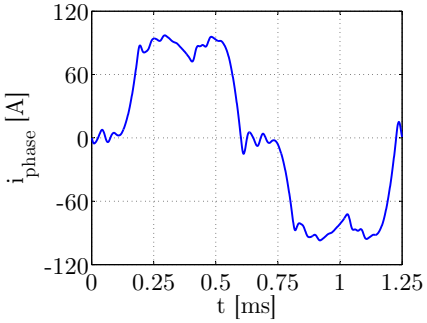


Figure 5.38: Phase current with additional parallel damping.

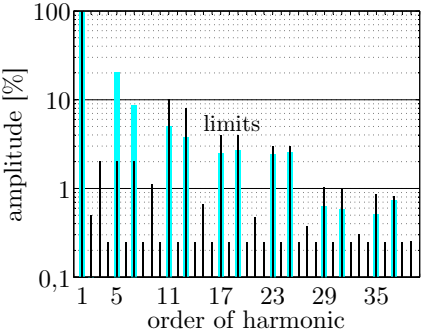


Figure 5.39: Spectrum of current in fig. 5.38.

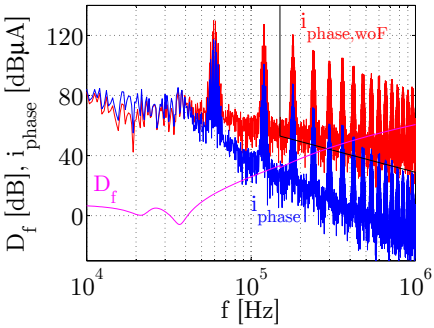


Figure 5.40: Ripple filter damping and spectrum of phase current with and without ripple filter according to fig. 5.37.

5.5.2 Common mode filter

The common-mode filter (fig. 5.1) consists of an LCL input filter and two C_y at the DC-link. Fig. 5.41 shows the equivalent CM model derived from the schematic in fig. 5.1. The common-mode (CM) voltage of the active filter (v_{cm2}) can be derived from the switching vectors generated in section chapter 5.5.1. Fig. 5.42 displays the CM voltage in time-domain, fig. 5.43 the corresponding spectrum. A realistic dv/dt of the edges (e.g. 10 kV/µs) has low impact in the calculated frequency range up to 10 MHz and is therefore not implemented. In this case the motor inverter acts as a further CM voltage source (v_{cm1}). The generation of this voltage is described in chapter 3.2. The C_y capacitance is chosen according to standard ABD0100 1.2 ([117]), which requires a minimal impedance between input phases and housing of 100 Ω at 10 kHz. With five C_y

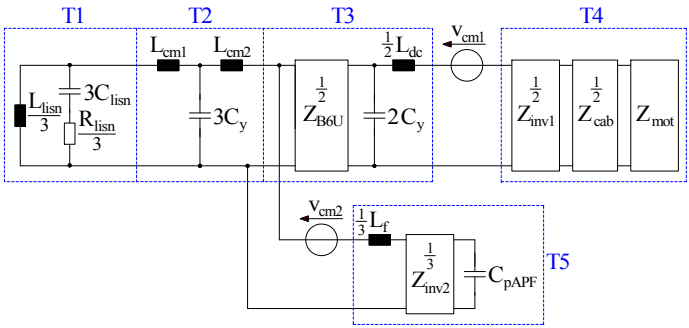


Figure 5.41: Equivalent model for the common-mode filter design.

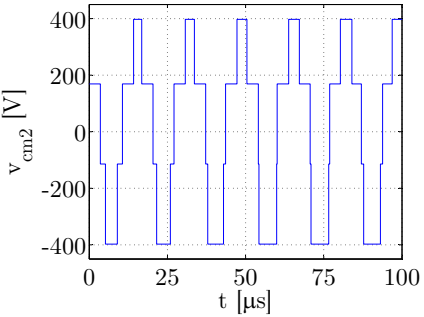


Figure 5.42: Common mode voltage of active filter in time domain.

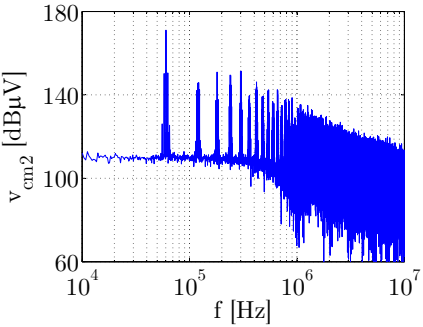


Figure 5.43: Spectrum of CM voltage in fig. 5.42.

capacitors, the maximum value for one C_y is:

$$C_{y,max} = \frac{1}{5 \cdot 100\Omega \cdot 2\pi \cdot 10kHz} \approx 32nF \tag{5.43}$$

The C_x and C_y capacitors are arranged in star topology to enable the use of capacitors with 1200 V_{dc} rating. The necessary voltage rating must be chosen according to the lightning and voltage spike requirements in standard [11]. In principle, the C_x capacitors may be arranged in Δ-topology, too. In this case, a voltage rating of at least 2 kV_{dc} is necessary. The impedances of rectifier (Z_{B6U}) and power modules (Z_{inv1}, Z_{inv2}) are measured by an impedance analyzer. Since the power modules have a passive behaviour from the point of view of a CM current, z_{11} and z_{22} are nearly identical and thus only the measurement of z_{11} and z_{sc} is necessary. The corresponding result for Z_{inv2} is depicted in fig. 5.44 and fig. 5.45. All measured impedances are modelled by a passive network to simplify the calculation of the entire CM model. The CM impedances of output cables and motor (Z_{cab} and Z_{mot}) are described in chapter 3.2.5. The parasitic capacitance of the IGBT driver boards and DC-link is estimated by the parallel-plate capacitance formula (eq. 5.44):

$$C_{pAPF} = 2\epsilon_0\epsilon_r \frac{A_f}{d_f} \tag{5.44}$$

with distance between PCB and housing d_f, total floating area A_f, $\epsilon_0 = 8.854\frac{H}{m}$ and $\epsilon_r = 1$. In the hardware, there are further parasitic capacitances to earth potential, e.g. to the left and right side of the boards. Furthermore, there is a shielding between controller board and IGBT drivers.

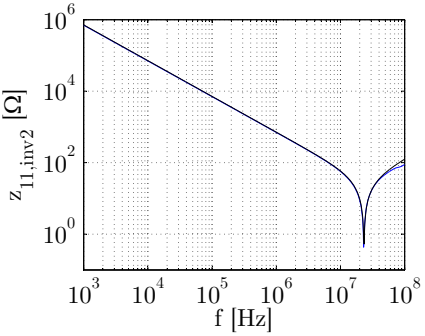


Figure 5.44: Measurement of input impedance $z_{11,inv2}$.

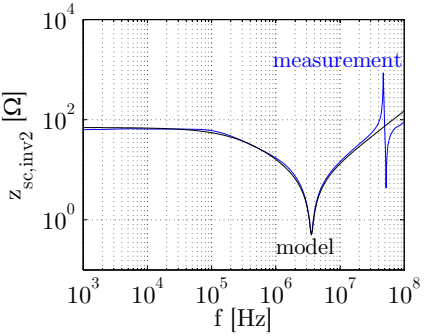


Figure 5.45: Measurement of short-circuit impedance $z_{sc,inv2}$.

To take into account these parasitics, a factor of two is included in eq. 5.44. The result is 68 pF, which is small compared to the IGBT-module with a z_{11} of 222 pF.

In this model, two CM voltage sources are present - duplex motor inverter and APF inverter. To calculate the resulting current through the input phases, the superposition principle is applied. First, v_{cm2} is short-circuited. The equivalent single-phase model is shown in fig. 5.46. The input impedance $Z_{5,11}$ is now parallel to the input impedance of $Z_{3,11}$. To simplify the calculation, $Z_{5,11}$ is transformed to an own transfer matrix T_5'.

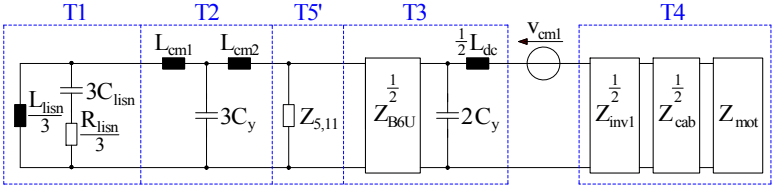


Figure 5.46: Equivalent CM model with short-circuited voltage v_{cm2}.

The equivalent model with summarized impedances changes according to fig. 5.47, where

$$Z_6 = \begin{bmatrix} \frac{T_{6,11}}{T_{6,21}} & T_{6,11}\frac{Z_{6,22}}{Z_{6,21}} - T_{6,12} \\ \frac{1}{T_{6,21}} & \frac{T_{6,22}}{T_{6,21}} \end{bmatrix} \tag{5.45}$$

with

$$T_6 = T_1 T_2 T_5' T_3. \tag{5.46}$$

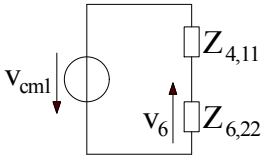


Figure 5.47: Equivalent model with short circuited source v_{cm2}.

Voltage v_6 (voltage at right hand side of T_6) can be calculated with the voltage divider formula:

$$v_6 = -\frac{Z_{6,22}}{Z_{4,11} + Z_{6,22}} v_{cm1} \tag{5.47}$$

The current into Z_6 is then:

$$i_6 = \frac{v_6}{Z_{6,22}} \tag{5.48}$$

With v_6 and i_6 the voltage across the LISN (T_1) can be derived according to fig. 5.48:

$$v_1 = T_{6,11} v_6 + T_{6,12} i_6 \tag{5.49}$$

To calculate the CM current without input filter ($i_{cm1,woF}$), the input filter represented by T_2 is deactivated by setting

$$T_2 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \tag{5.50}$$

The resulting CM current $i_{cm1,woF}$ into the supply is then calculated through

$$i_{cm1,woF} = \frac{v_1}{Z_{1,22}}. \tag{5.51}$$

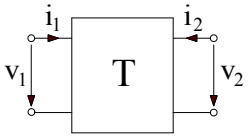


Figure 5.48: Input and output definition of one transfer matrix.

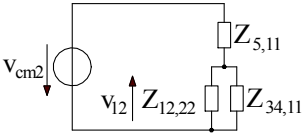


Figure 5.49: Equivalent model with short circuited source v_{cm1}.

The second step is the short-circuit of v_{cm1}. The resulting impedance model is shown in fig. 5.49 with summarized matrices

$$T_{12} = T_1 T_2 \tag{5.52}$$

and

$$T_{34} = T_3 T_4. \tag{5.53}$$

From the point of view of v_{cm2}, impedances $Z_{12,22}$ and $Z_{34,11}$ are parallel. Together with Z_5, the schematic in fig. 5.49 can be derived. Voltage v_{12} can be calculated again using the voltage divider approach:

$$v_{12} = -\frac{Z_{12,22} Z_{34,11}}{Z_{5,11}\left(Z_{12,22} + Z_{34,11}\right) + Z_{12,22} Z_{34,11}} v_{cm2} \tag{5.54}$$

The input current i_{12} at the right hand side of T_{12} is

$$i_{12} = \frac{v_{12}}{Z_{12,22}}. \tag{5.55}$$

With v_{12} and i_{12} the voltage at the left hand side of T_{12} can be calculated through

$$v_{12,left} = v_1 = T_{12,11} v_{12} + T_{12,11} i_{12}, \tag{5.56}$$

where v_1 is the right hand side voltage of T_1. $v_{12,left}$ and v_1 are identical, since the LISN (T_1) does not have a voltage divider between right hand and left hand side voltage. The CM current without input filter $i_{cm2,woF}$ is then

$$i_{cm2,woF} = \frac{v_1}{Z_{1,22}} = \frac{T_{12,11} v_{12}}{Z_{1,22}} + \frac{T_{12,12} v_{12}}{Z_{1,22} Z_{12,22}}. \tag{5.57}$$

The total CM current without input filter ($i_{cm,woF}$) is the sum of $i_{cm1,woF}$ and $i_{cm2,woF}$:

$$i_{cm,woF} = i_{cm1,woF} + i_{cm2,woF} \tag{5.58}$$

The calculations from eq. 5.45 to eq. 5.57 have to be performed for every single frequency in the required range. The results for $i_{cm1,woF}$ and $i_{cm2,woF}$ are depicted in fig. 5.50 and fig. 5.51. Up to 150 kHz, $i_{cm1,woF}$ is above $i_{cm2,woF}$. From 150 kHz to 10 MHz, the active filter noise is dominating. At e.g. 1 MHz, a the input filter must have an insertion damping of at least 70 dB. Since C_y is already defined, only the value of the common-mode chokes has to be determined. To avoid the specification and purchasing of two different chokes, L_{cm1} and L_{cm2} are set to be equal.

To determine the necessary value L_{cm} for the two common-mode chokes,

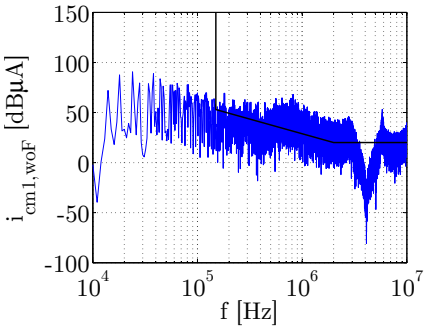


Figure 5.50: CM current $i_{cm1,woF}$ caused by v_{cm1} (without filter).

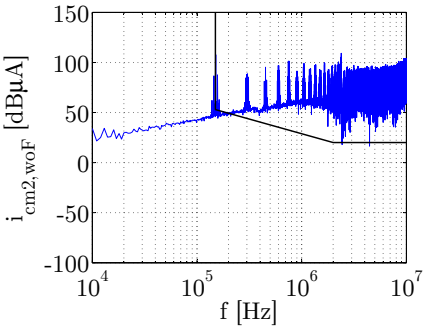


Figure 5.51: CM current $i_{cm2,woF}$ caused by v_{cm2} (without filter).

the damping without input filter $D_{cm,woF}$ has to be defined first:

$$D_{cm,woF} = \left|\frac{v_{cm2}}{v_1}\right| = \left|\frac{Z_{5,11}\left(Z_{1,22} + Z_{34,11}\right) + Z_{1,22}Z_{34,11}}{Z_{1,22}Z_{34,11}}\right| \tag{5.59}$$

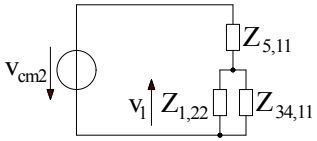


Figure 5.52: Simplified model for damping calculation.

This is done using the simplified model in fig. 5.52, where only v_{cm2} is taken into account. v_{cm1} is negligible at frequencies above 150 kHz, since the CM current $i_{cm1,woF}$ is lower than $i_{cm2,woF}$. For the calculation of the damping with filter D_{cm}, input filter Z_2 is included by using Z_{12} instead of Z_1 in the damping formula:

$$D_{cm} = \left|\frac{v_{cm2}}{v_1}\right| = \left|\frac{Z_{5,11}\left(Z_{12,22} + Z_{34,11}\right) + Z_{12,22}Z_{34,11}}{Z_{12,22}Z_{34,11}}\right| \tag{5.60}$$

At 1 MHz, the insertion damping of T_2 should be 70 dB, i.e. D_{cm} should be 70 dB above $D_{cm,woF}$. This is expressed by

$$D_{cm,woF} + 70dB - D_{cm} = 0. \tag{5.61}$$

An analytical calculation of L_{cm} is theoretically possible, but the resulting formula derived from eq. 5.61 is long and therefore eq. 5.61 is solved nu-

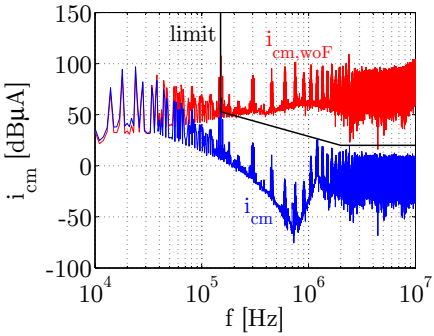


Figure 5.53: CM current spectrum with (i_{cm}) and without input filter.

merically. The entire CM model is then calculated again with the resulting value for L_{cm} and the proposed value for C_y. The comparison between the total CM current with and without input filter is displayed in fig. 5.53. The maximum damping is a achieved at about 800 kHz. At frequencies above 800 kHz, the impedance of the CM chokes decreases due to the parasitic capacitance and therefore the damping cannot further increase.

6 Analysis and design of control algorithm

6.1 Main structure

The current control algorithm has to be robust and accurate during steady state conditions. During frequency steps or ramps, the active filter must remain stable and follow with reasonable compensation performance but without faults or loss of control. To cope with both requirements, the control algorithm (fig. 6.1) consists of two parts. The basic APF operation

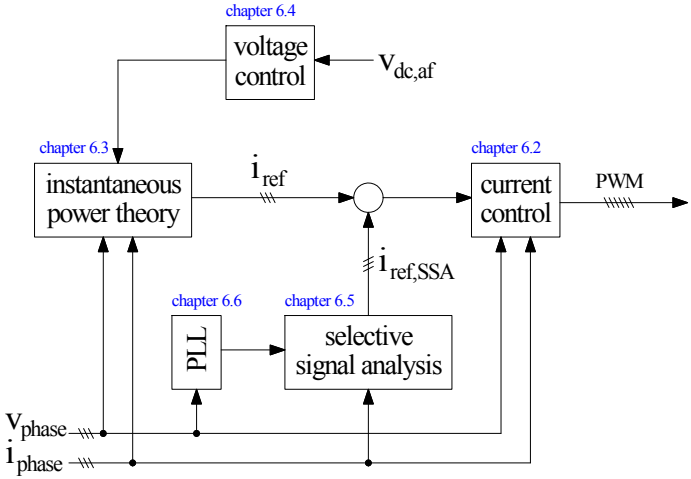


Figure 6.1: Proposed two-stage algorithm with fundamental reference current generation through the instantaneous power theory and harmonic control through the selective signal analysis.

is performed by the current control (chapter 6.2), voltage control (chapter 6.4) and fundamental reference current generation based on instantaneous power theory (chapter 6.3). The instantaneous power calculation does not require a line synchronization and therefore offers a very high robustness. The second part consists of the selective signal analysis (SSA) (chapter 6.5) and a phase locked loop for line synchronization (chapter 6.6). Due to the

small filter inductances L_f, the current control gain is small (eq. 6.17). Without SSA, the resulting compensation performance is not sufficient (fig. 6.10). Hence, the SSA is necessary to achieve the required accuracy of less then 2% for the 5^{th} and 7^{th} harmonics.

The error amplifier is realized by a P current controller, which is supported by a voltage feed forward. The switching frequency f_{sw} and the sample frequency f_s are 60 kHz with periods

$$T_s = \frac{1}{f_s} \tag{6.1}$$

and

$$T_{sw} = \frac{1}{f_{sw}}. \tag{6.2}$$

According to the requirements, the three phase currents i_{phase} shall be used for the APF control. The rectifier and compensation currents are not measured. Furthermore, the three phase-to-phase input voltages and the APF DC-link voltage are measured.

6.2 Analysis of current control loop

A functional diagram of the current control loop is depicted in fig. 6.2 with transfer functions G_c for the control, G_{inv} for the inverter, G_{AD} for the analogue-to-digital conversion, G_f for the ripple filter and G_p for the total hardware process. According to [118], a digital system can be approximated by multiplying the continuous transfer function with a dead time T_D of half the sample time T_s. This approximation is valid, if f_s is at least 6 times above the highest relevant system frequency f_{max}. This is expressed by

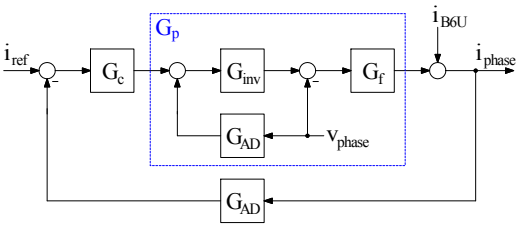


Figure 6.2: Structure of proposed current controller.

$$\frac{f_s}{f_{max}} \geq 6 \tag{6.3}$$

In this application, f_{max} is the 7^{th} harmonic of the 800 Hz supply (5,6 kHz) and the sampling as well as the switching frequency is 60 kHz. Hence, this

approximation is valid and T_D is added to the inverter dead time (eq. 6.5). The inverter stage with NPT-IGBTs is considered to be linear, but with a delay of

$$T_{inv} = 1{,}5T_{sw}. \tag{6.4}$$

This is a common approach. One period T_{sw} is due to the sampling and a further $\frac{1}{2}T_{sw}$ is necessary, until the new inverter output voltages have an effect. The total delay T_t is

$$T_t = T_D + T_{inv} = 2{,}0T_{sw} \tag{6.5}$$

To avoid the use of a non-linear dead time, delay T_t is approximated by a 1st order low-pass filter. As described in [119], the area between step responses of dead time and its approximation in the range from 0 to ∞ seconds must be zero. Considering this requirement, the equivalent time constant of the low-pass filter is equal to the dead time. The transfer function comprising delay T_t is then

$$G_{inv} = \frac{1}{1 + sT_t}. \tag{6.6}$$

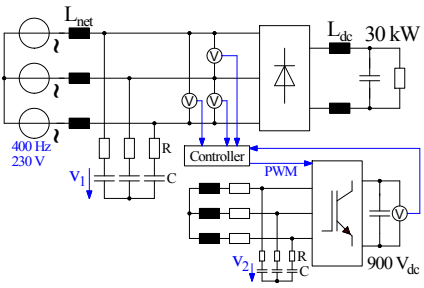


Figure 6.3: Test setup to derive linearity, gain and delay of APF inverter stage.

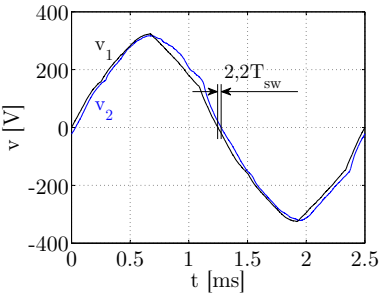


Figure 6.4: Measurement of v_1 and v_2 according to fig. 6.3. The delay of inverter output voltage v_2 is about $2.2T_{sw}$.

To verify the assumption of $T_t = 2.0T_{sw}$, a measurement according to fig. 6.3 is performed. The APF is disconnected from the main power supply and powered by a DC-source. The APF controller measures the phase-to-phase voltages and calculates the phase-to-neutral voltage. This voltage is reproduced by the APF inverter. The RL-load is necessary to drive the inverter in a realistic condition. A simple RC filter is applied to filter the switched voltages. v_1 and v_2 are measured with an oscilloscope (fig. 6.4). Since v_1 is filtered by an RC filter with equal parameters, the phase shift

at 400 Hz is equal for v_1 and v_2 and can be therefore neglected. The gain error between v_1 and v_2 is compensated for in software. The phase shift is about $2.2T_{sw}$, which is not so far from the assumption of $2.0T_{sw}$. For further analysis, $2.2T_{sw}$ is used.

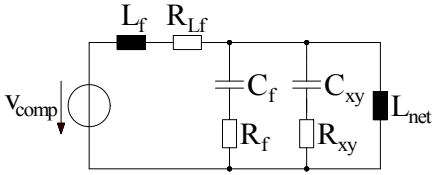


Figure 6.5: Simplified model of the control process.

The simplified model of the ripple filter shown in fig. 6.5. The ripple filter consists of a single-stage LCR topology (L_f, C_f and R_f). R_{Lf} is the ohmic resistance of L_f. The filter capacitors C_f and C_{xy} are not taken into consideration, since the dominant time constant is defined through the inductors. Hence, the transfer function G_{f1} can be modelled through a first-order low-pass filter comprising filter inductor L_f, source inductance L_{net} and R_{Lf} as ohmic resistance of L_f:

$$G_{f1} = \frac{\frac{1}{R_{Lf}}}{1 + s\frac{L_{APF}}{R_{Lf}}} \tag{6.7}$$

with total control relevant inductance $L_{APF} = L_f + L_{net}$. G_{AD} is negligible, since the analogue-to-digital conversion time in the DSP is in the range of 100 ns and the discretization is already considered by T_D. Furthermore, the sensors have a bandwidth of at least 60 kHz, which corresponds to a delay of about $0.16T_{sw}$. Compared to the T_t of $2.2T_{sw}$, this influence is negligible.

The complete process transfer function G_{p1} consists of G_{inv} and G_{f1}:

$$G_{p1} = \frac{\frac{1}{R_{Lf}}}{(1 + s\frac{L_{APF}}{R_{Lf}})(1 + sT_t)} \tag{6.8}$$

This second-order low-pass filter has a dominant time constant ($\frac{L_{APF}}{R_{Lf}}$), which enables the compensation by a PI-controller with transfer function

$$G_{c1} = K_{cc}\frac{1 + sT_i}{sT_i}, \tag{6.9}$$

where K_{cc} is the gain and T_i the integral time constant. The complete

closed-loop function is

$$G_{cc1} = \frac{G_{c1}G_{p1}}{1 + G_{c1}G_{p1}} = \frac{\frac{\frac{K_{cc}}{R_{Lf}}(1+sT_i)}{sT_i(1+s\frac{L_{APF}}{R_{Lf}})(1+sT_t)}}{1 + \frac{\frac{K_{cc}}{R_{Lf}}(1+sT_i)}{sT_i(1+s\frac{L_{APF}}{R_{Lf}})(1+sT_t)}}. \tag{6.10}$$

By setting T_i to

$$T_i = \frac{L_{APF}}{R_{Lf}}, \tag{6.11}$$

the terms $1 + s\frac{L_{APF}}{R_{Lf}}$ cancel each other out and G_{cc1} is simplified to

$$G_{cc1} = \frac{\frac{\frac{K_{cc}}{R_{Lf}}}{s\frac{L_{APF}}{R_{Lf}}(1+sT_t)}}{1 + \frac{\frac{K_{cc}}{R_{Lf}}}{s\frac{L_{APF}}{R_{Lf}}(1+sT_t)}} = \frac{1}{1 + s\frac{L_{APF}}{K_{cc}} + s^2\frac{L_{APF}T_t}{K_{cc}}}. \tag{6.12}$$

If the dominant time constant in G_p is unknown or has high tolerances, the compensation is not possible. In this case, the filter inductance L_f has a typical tolerance of about $\pm 20\%$. Furthermore, the source inductance L_{net} is only valid for laboratory experiments. The real inductance of generator and cables in the aircraft is unknown. Hence, the first approach with the PI-controller and the compensation of time constant cannot be applied.
The second approach uses a P-controller and considers a purely integral behaviour of the ripple filter. The transfer function of the controller is then

$$G_{c2} = K_{cc} \tag{6.13}$$

and the ripple filter function is

$$G_{f2} = \frac{1}{sL_{APF}}. \tag{6.14}$$

The process function is defined by

$$G_{p2} = \frac{1}{sL_{APF}(1 + sT_t)}. \tag{6.15}$$

The resulting closed loop transfer function

$$G_{cc2} = \frac{G_{c2}G_{p2}}{1 + G_{c2}G_{p2}} = \frac{1}{1 + s\frac{L_{APF}}{K_{cc}} + s^2\frac{L_{APF}T_t}{K_{cc}}} \tag{6.16}$$

is identical to G_{cc1}. For the further design process, the second solution with a pure P-controller is used. The dependency of K_{cc} on the desired damping D_{cc} is

$$K_{cc} = \frac{L_{APF}}{4D_{cc}^2 T_t} \tag{6.17}$$

(chapter A.1.3). To get the best reference-variable response of the control system, damping D_{cc} is set to $\frac{1}{\sqrt{2}}$ (optimum amount criterium). As shown in fig. 5.3, the value of L_f is very small. Hence, the current control gain K_{cc} is small, too, which leads to a high systematic control error. The result is an insufficient compensation quality as described in the following section.

6.3 Reference current generation with instantaneous power theory

A very common methodology for deriving reference currents in an active power filter application is based on the instantaneous power theory (fig. 6.6, [120], [121], [122]).

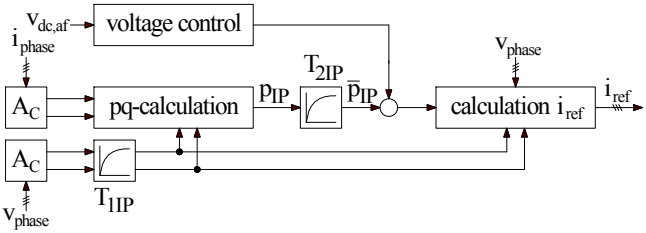


Figure 6.6: Reference current generation based on instantaneous power theory.

Phase voltages and currents are transformed into the static $\alpha - \beta$ coordinate system through

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} [A_C] \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{6.18}$$

and

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}}[A_C] \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \tag{6.19}$$

with Clarke transformation matrix A_C. The instantaneous real and imaginary power are calculated using

$$\begin{bmatrix} p_{IP} \\ q_{IP} \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}. \tag{6.20}$$

The reference currents are calculated through

$$\begin{bmatrix} i_{a,ref} \\ i_{b,ref} \\ i_{c,ref} \end{bmatrix} = \frac{\bar{p}_{IP}}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{6.21}$$

with low-pass filtered real power $\bar{p}_{IP}$. Due to the distorted voltage and current waveforms, the resulting power has a ripple. This ripple has a frequency of six times the supply frequency and is damped using a first order low-pass filter with time constant T_{2IP}. The time constant T_{2IP} (chapter A.1.5) is defined by the desired damping D_{2IP} of the 6^{th} harmonic at 360 Hz supply frequency:

$$T_{2IP} = \sqrt{\frac{D_{2IP} - 1}{\omega_6^2}} \tag{6.22}$$

with $\omega_6 = 6 \cdot 2\pi \cdot 360Hz$.

Optionally, a second low-pass filter T_{1IP} can be implemented to dampen high frequency components in v_{net}. In this proposed control algorithm, low-pass filter T_{1IP} is not implemented. Fig. 6.7 shows simulated phase voltage and current during full power operation with diode bridge rectifier. The step response of $\bar{p}_{IP}$ is depicted in fig. 6.8.

The derived reference current during diode bridge operation is shown in fig. 6.9. Fig. 6.10 compares reference current and achieved phase current during compensation. The compensation quality is not sufficient due to the small current control gain K_{cc}. To ensure the requirement on compensation accuracy, the basic control algorithm with instantaneous power theory must be extended by an additional control component - the selec-

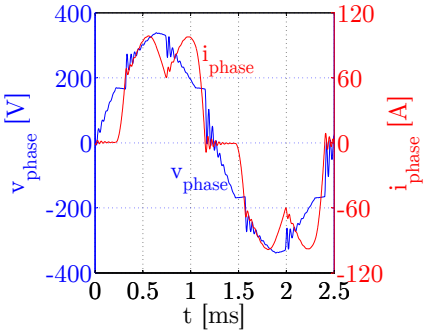


Figure 6.7: Distorted phase voltage and phase current during diode bridge operation.

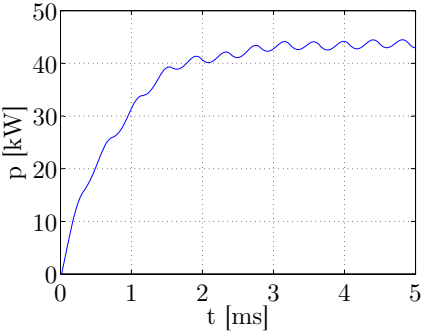


Figure 6.8: Step response of filtered instantaneous power $\bar{p}$ during diode bridge operation.

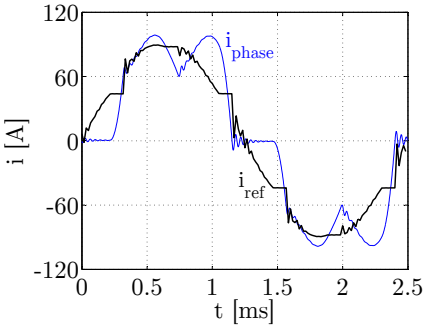


Figure 6.9: Reference current calculated with eq. 6.21 without compensation.

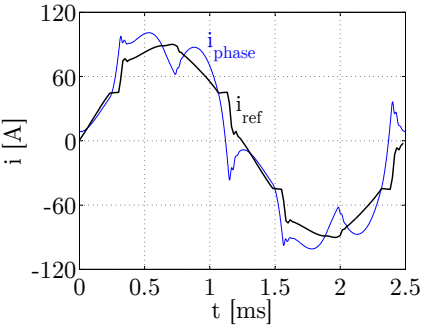


Figure 6.10: Derived reference current and phase current during compensation.

tive signal analysis (SSA) (fig. 6.1), which is described in chapter 6.5.

The delay of the instantaneous power calculation caused by time constant T_{2IP} charges the APF DC-link during a full load dump. Considering an error (e.g. an over-temperature in the duplex motor), the PWM signals of the main inverter are deactivated automatically by a hardware circuit. This results in a very fast power drop from nominal power P_{nom} to zero and is expressed by

$$p_{load}(t) = \frac{P_{nom}}{2}\big(1 - sgn(t)\big). \tag{6.23}$$

Due to the low pass filter T_{2IP}, the calculated instantaneous power $p_{IP}(t)$ in the APF controller has a delay (fig. 6.11) and is described by

$$p_{IP}(t) = P_{nom} e^{-\frac{t}{T_{2IP}}} \tag{6.24}$$

for $t \geq 0\ s$. The difference between real power $p_{load}(t)$ and calculated power $p_{IP}(t)$ is named $p_z(t)$ and defined as

$$p_z(t) = p_{IP}(t) - p_{load}(t) = P_{nom} e^{-\frac{t}{T_{2IP}}} \tag{6.25}$$

for $t \geq 0\ s$. Without voltage control, the power difference respectively power disturbance $p_z(t)$ charges the DC-link to

$$V_{dc,wC} = \sqrt{\frac{2 P_{nom} T_{2IP}}{C_{dc,af}} + V_{ref}^2} \tag{6.26}$$

with APF DC-link capacitance $C_{dc,af}$ and reference DC-link voltage V_{ref} (chapter A.1.6). Since P_{nom} and V_{ref} are fixed, the resulting DC-link voltage depends on $C_{dc,af}$ and T_{2IP} only. The loss of control can occur if the voltage sensor has an error or runs into saturation.

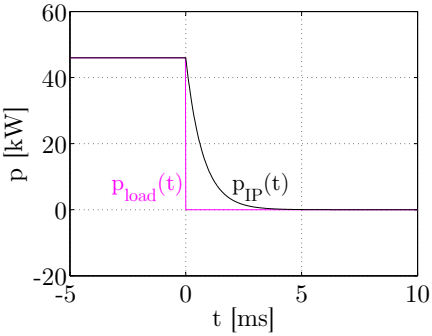


Figure 6.11: Load dump at occurrence of an error and calculated power by instantaneous power theory.

The power characteristic during E-ECS start-up is not critical, since the motor ramps up to full power within 2 s (chapter 2.4). Hence, only the load dump is considered for the design of voltage control algorithm in the following section.

6.4 Voltage control of APF DC-link

The schematic of the voltage control loop is depicted in fig. 6.12. APF inverter, inductances and other delays are not taken into account, since the dominant time constant in the process is caused by the APF DC-link capacitance $C_{dc,af}$. G_{VC} represents the PID-T_1 controller, G_{pVC} the process with $C_{dc,af}$. The reference voltage V_{ref} is smoothed by a low-pass filter with time constant T_{1VC}. Since the reference voltage is not changed during the normal APF operation, this time constant is not critical and is set to 50 ms at all simulations and laboratory measurements.

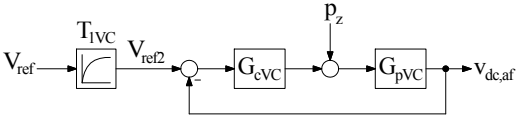


Figure 6.12: Schematic of voltage control loop.

The DC-link voltage is adjusted by adding positive or negative power to the calculated instantaneous power (fig. 6.6), i.e. the output of G_{VC} is a power. The disturbance power p_z is caused by the delay of instantaneous power calculation during a load dump (see previous section). The most important task of the APF voltage control is the overvoltage protection during this load dump.
The voltage of a capacitance, which is charged by a constant power P, has a non-linear characteristic with

$$v_C(t) = \sqrt{\frac{2P}{C_{dc,af}}t} \tag{6.27}$$

(fig. 6.13). That is why a linearization at the working point is necessary before applying the standard analysis methods with Laplace transfer functions. The linearized function at V_{ref} is defined by

$$v_{C,lin}(t) = \frac{P}{V_{ref}C_{dc,af}}t + \frac{1}{2}V_{ref} \tag{6.28}$$

and depicted in fig. 6.13.

The main time constant in the process is caused by $C_{dc,af}$. The influence of inductors, inverter and sensors are negligibly small. The process transfer function can then be defined as

$$G_{pVC} = \frac{1}{sV_{ref}C_{dc,af}}. \tag{6.29}$$

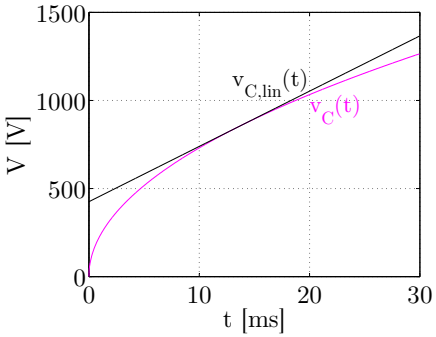


Figure 6.13: Voltage v_C at $C_{dc,af}$ when charged with constant power of 2 kW and linearization at operating point V_{ref}.

As control topology, a classical PID-T_1 type is applied:

$$G_{cVC} = K_{pVC} + \frac{1}{T_{iVC}s} + \frac{sT_{dVC}}{sT_{2VC}+1} \tag{6.30}$$

The resulting reference and disturbance transfer functions are defined by

$$G_{VC} = \frac{\big(T_dT_i + K_pT_iT_2\big)s^2 + \big(K_pT_i + T_2\big)s + 1}{T_iT_2V_{ref}C_{dc,af}s^3 + \big(T_iV_{ref}C_{dc,af} + T_dT_i + K_pT_iT_2\big)s^2 + ... \\ \overline{+\big(K_pT_i + T_2\big)s + 1}} \tag{6.31}$$

and

$$G_{zVC} = \frac{T_iT_2s^2 + T_is}{T_iT_2V_{ref}C_{dc,af}s^3 + \big(T_iV_{ref}C_{dc,af} + T_dT_i + K_pT_iT_2\big)s^2 + ... \\ \overline{+\big(K_pT_i + T_2\big)s + 1}}. \tag{6.32}$$

The index "VC" at the parameters is omitted for reasons of clarity and readability.
The P-component alone should be able to reduce the steady-state control error to less than 2 % considering the necessary charging power P_{loss} (P_{loss} are mainly the inverter losses). Thus, the minimum required value for

K_{pVC} can be calculated through

$$K_{pVC} = \frac{P_{loss}}{0.02 V_{ref}}. \tag{6.33}$$

The integral component is important only for tracking the low-pass filtered reference voltage V_{ref2}. The differential part is important only for disturbances such as the load dump. Thus, the differential component is not taken into account for the design of integral component. The resulting closed-loop reference transfer function is

$$G_{iVC} = \frac{1 + K_{iVC} T_{iVC} s}{1 + K_{iVC} T_{iVC} s + T_{iVC} V_{ref} C_{dc,af} s^2}. \tag{6.34}$$

Without the term $K_{iVC} T_{iVC} s$ in the nominator, G_{iVC} would be a second-order low-pass filter. If a second-order low-pass filter consists of two first-order low-pass filters in series, the resulting step response shows no overshoot. This criterium is used for G_{iVC}:

$$G_{iVC} = \frac{1 + K_{iVC} T_{iVC} s}{(1 + T_{VC} s)^2} = \frac{1 + K_{iVC} T_{iVC} s}{1 + 2 T_{VC} s + T_{VC}^2 s^2} \tag{6.35}$$

with

$$T_{VC} = \frac{2 V_{ref} C_{dc,af}}{K_{pVC}}. \tag{6.36}$$

By coefficient comparison, the formula for the necessary integral time constant T_i is developed to

$$T_i = \frac{4 V_{ref} C_{dc,af}}{K_{pVC}^2}. \tag{6.37}$$

The low pass filter with T_{2VC} dampens the high frequency noise to avoid additional disturbances by the D-component in G_{cVC}. In this application, the switching and sampling frequency at $f_{sw} = 60\ kHz$ is the main noise source. The time constant is calculated using

$$T_{2VC} = \sqrt{\frac{D_{2VC}^2 - 1}{(2\pi f_{sw})^2}} \tag{6.38}$$

where D_{2VC} is the desired damping at f_{sw}. For the design of D-component time constant T_{dVC}, G_{VC} with open control loop (G_{oVC}) is considered. If the disturbance shown in fig. 6.11 occurs, the short time peak power into

the APF DC-link is 46 kW. The maximum output of the D-T_1 element shall be 46 kW, too. With G_{oVC} and low pass filter T_{2VC}, the maximum value of time constant T_{dVC} can be calculated:

$$T_{dVC,max} = V_{ref} C_{dc,af} \left(\frac{1}{2} + T_{2VC} f_s \right) \tag{6.39}$$

For a first evaluation of the voltage controller, the damping D_{2VC} is set to 40 dB and T_{dVC} is set to $0{,}1 T_{dVC,max}$. However, both the time constant T_{2VC} and T_{dVC} are strongly dependent on the noise of real application and have to be optimized in the prototype.
The response of G_{VC} on the filtered reference voltage V_{ref2} is depicted in fig. 6.14. The behaviour is excellent, since the time constant of G_{iVC} is significantly smaller than the 50 ms, which are used for time constant T_{1VC}.

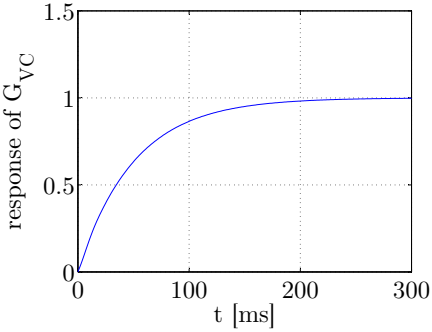


Figure 6.14: Response of G_{VC} on V_{ref2}. V_{ref2} is not plotted, since there is nearly no difference to the G_{VC} response.

The disturbance $p_z(t)$ caused by the load dump and the behaviour of controlled DC-link voltage (G_{zVC}) are depicted in fig. 6.15. The voltage overshoot is about 120 V, which is not critical for 1700 V power semiconductors. The D-component could be increased, since the PID-T_1 control stage has a maximum output $p_C(t)$ of about 24 kW only (fig. 6.16).

The low-frequency DC-link ripple (fig. 5.4) is caused be the generation of harmonics and cannot be avoided. If the voltage control compensates for this ripple, it would work against the current control. That is why the insertion damping of G_{cVC} shall be as small as possible at the 6^{th} harmonic of the lowest supply frequency 360 Hz (2160 Hz). Fig. 6.17 displays a comparison between G_{pVC} and G_{zVC}. At 2160 Hz the difference is 1.7 dB, which is very small. Furthermore, the simulation results in chapter 6.7 do not show any negative effects due to the voltage control.

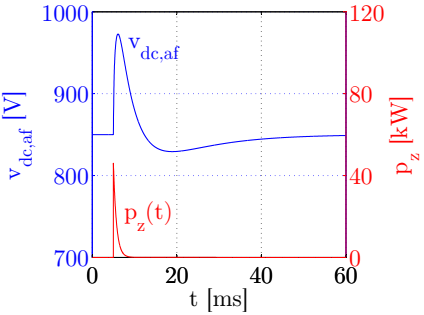


Figure 6.15: DC-link voltage and power p_z into DC-link voltage at load dump.

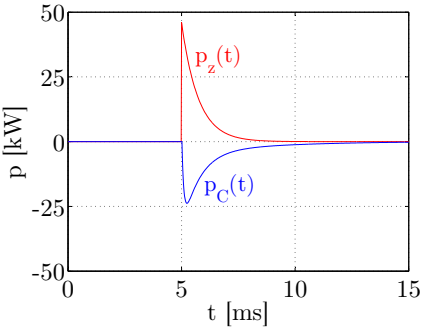


Figure 6.16: Disturbance power p_z and output of PID-T_1 controller p_C.

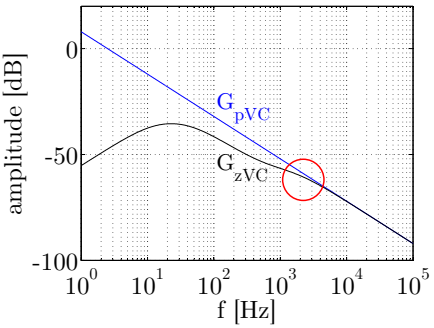


Figure 6.17: Amplitude vs. frequency of G_{pVC} and G_{zVC}. At 2160 Hz (6^{th} harmonic of 360 Hz) the voltage control causes only 1.7 dB additional damping.

6.5 Design of selective signal analysis

As described in chapter 6.3, the basic control algorithm with instantaneous power is extended by a harmonic analysing component (fig. 6.1). There are several methods to analyse a signal for certain frequency components. The digital Fourier transform (DFT) is supported by many signal processors, but can only be calculated cyclically, requiring interrupts and harmonics management. The rotating dq-frame method is very common, but offers little flexibility, since all three phases are calculated simultaneously. This is critical, especially in applications with high switching frequencies, since the available processing time of the digital signal processor (DSP) is limited. Both disadvantages can be avoided by applying the selective signal

analysis (SSA) [88] as shown in fig. 6.18. The SSA continuously analyses

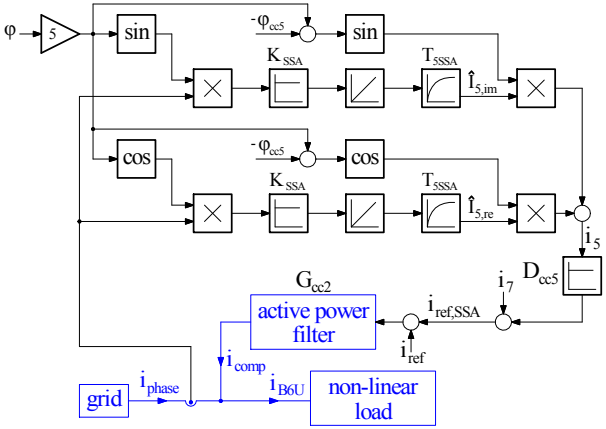


Figure 6.18: Selective signal analysis of one phase current for the 5^{th} harmonic. The blue parts are hardware components.

the phase currents for complex components of the 5^{th} and 7^{th} harmonics. These components are low pass filtered, transformed into sinusoidal signals added to the existing reference current i_{ref}. Hence, the generated compensation current i_{comp} changes according to $i_{ref,SSA}$ and reduces the harmonic content of i_{phase}. The integral behaviour of the SSA varies the real and imaginary components of the analysed current harmonic until the corresponding content in i_{phase} is zero.

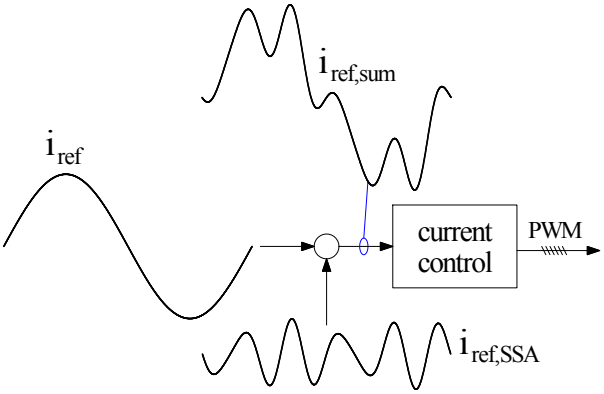


Figure 6.19: Reference current i_{ref}, SSA reference current $i_{ref,SSA}$ and total reference current $i_{ref,sum}$.

Fig. 6.19 clarifies the function of the SSA. The basic reference current i_{ref} consisting of the fundamental only is calculated by the instantaneous

power theory. The SSA adds $i_{ref,SSA}$ consisting of the 5$^{\text{th}}$ and 7$^{\text{th}}$ harmonics on i_{ref}. This sum ($i_{ref,sum}$) is fed into the current controller.
Since the basic active filter operation is always ensured by the instantaneous power algorithm, the SSA dynamics are not critical. Therefore, the number of phases and harmonics, which are analysed simultaneously, can be chosen dependent on the available processing power of the controller. The slowest solution is to multiplex the four signals (2 times 5$^{\text{th}}$, 2 times 7$^{\text{th}}$), e.g. while analysing phase A on 5$^{\text{th}}$ harmonic, the other three amplitudes remain constant. The next signal is the 5$^{\text{th}}$ harmonic in phase B, then 7$^{\text{th}}$ harmonic in phase A and 7$^{\text{th}}$ harmonic in phase B. Since there is no neutral phase, the correction current of phase C is calculated by the law of Kirchhoff. The multiplex approach has been successfully tested in simulation and prototype.
The mathematical description of the 5$^{\text{th}}$ harmonic without low pass filters and APF inverter is described by

$$i_{ref,SSA}(t) = K_{SSA}\Big[\sin(5\omega_{net}t)\int\Big(i_{phase}(t)\sin(5\omega_{net}t)dt\Big)+ \cos(5\omega_{net}t)\int\Big(i_{phase}(t)\cos(5\omega_{net}t)dt\Big)\Big]. \tag{6.40}$$

Until the content of 5$^{\text{th}}$ harmonic in i_{phase} is unequal zero, the integrators increase or reduce the real and imaginary components ($\hat{I}_{5,re}$ and $\hat{I}_{5,im}$). The amplitude of the 5$^{\text{th}}$ harmonic is defined by

$$\hat{I}_5 = \sqrt{\hat{I}_{5,re}^2 + \hat{I}_{5,im}^2}. \tag{6.41}$$

The following algorithm analysis is described for the 5$^{\text{th}}$ harmonic. The formulas for the 7$^{\text{th}}$ harmonic are analogous. The behaviour of the 5$^{\text{th}}$ harmonic is evaluated by the amplitude $\hat{I}_5$ (fig. 6.20).
The biggest amplitude, which must be damped by low-pass filter T_{5SSA} is the 6$^{\text{th}}$ harmonic. Hence, time constant T_{5SSA} is defined by the desired damping at the lowest supply frequency of 360 Hz:

$$T_{5SSA} = \sqrt{\frac{D_{5SSA}^2 - 1}{\omega_6^2}} \tag{6.42}$$

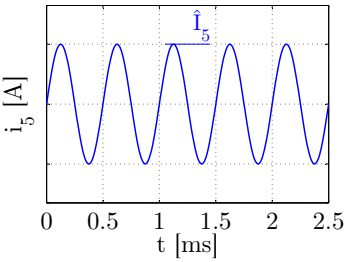


Figure 6.20: 5$^{\text{th}}$ harmonic in time domain (i_5) at 400 Hz. The amplitude is named $\hat{I}_5$.

with $\omega_6 = 6 \cdot 2\pi \cdot 360Hz$. Considering an ideal behaviour of the APF inverter ($G_{cc2} = 1$), the characteristic of the amplitude of 5$^{\text{th}}$ harmonic can be expressed as the transfer function

$$G_{5SSA} = \frac{1}{1 + s\frac{2}{K_{SSA}} + s^2\frac{T_{5SSA}}{K_{SSA}}} \tag{6.43}$$

The standard form for this transfer function is

$$G_{5SSA} = \frac{1}{1 + s2D_{SSA}T_{SSA} + s^2T_{SSA}^2} \tag{6.44}$$

with

$$T_{SSA} = 2T_{5SSA}D_{5SSA}. \tag{6.45}$$

By efficient comparison between eq. 6.43 and eq. 6.44, gain K_{SSA} (valid for 5$^{\text{th}}$ and 7$^{\text{th}}$ harmonic) can be determined through

$$K_{SSA} = \frac{1}{2D_{SSA}^2T_{5SSA}}. \tag{6.46}$$

For the first design, the optimum amount criterium with $D_{SSA} = \frac{1}{\sqrt{2}}$ is chosen. This value is valid for the transfer function of 7$^{\text{th}}$ harmonic, too. The influence of T_{5SSA}, respectively D_{5SSA}, on the step response of the amplitude of the 5$^{\text{th}}$ harmonic is depicted in fig. 6.21. The steady-state condition is reached after about 20 ms.

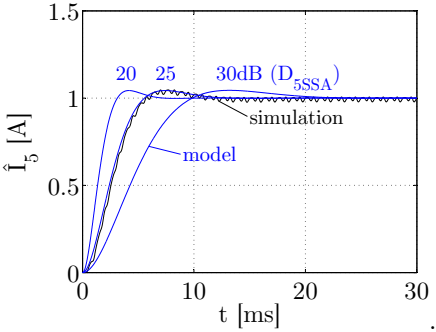


Figure 6.21: Step responses of amplitude of 5$^{\text{th}}$ harmonic for different values of D_{5SSA}.

Considering the real behaviour of the APF inverter with G_{cc2} in eq. 6.16, the low-pass filter characteristic of G_{cc2} has to be taken into account. The 5$^{\text{th}}$ harmonic current $i_5(t)$ is damped and phase shifted by G_{cc2}. The

damping of G_{cc2} at the 5$^{\text{th}}$ harmonic is calculated through

$$D_{cc5} = \left|\frac{1}{G_{cc2}(j\omega_5)}\right| = \sqrt{\left(1-\omega_5^2\frac{L_{APF}T_t}{K_{cc}}\right)^2 + \left(\omega_5\frac{L_{APF}}{K_{cc}}\right)^2} \tag{6.47}$$

and the phase shift through

$$\varphi_{cc5} = arg\big(G_{cc2}(j\omega_5)\big) = -\arctan\left(\frac{1}{\frac{K_{cc}}{\omega_5 L_{APF}} - \omega_5 T_t}\right) \tag{6.48}$$

with $\omega_5 = 5{\cdot}2\pi{\cdot}400Hz$. Especially the phase shift φ_{cc5} has a big impact on the SSA transfer function G_{5SSA}. Taking into account φ_{cc5}, the behaviour of 5$^{\text{th}}$ is determined by

$$G_{5SSA2} = \frac{D_{cc5}}{1 + s2D_{SSA}T_{SSA2} + s^2T_{SSA2}^2} \tag{6.49}$$

with

$$T_{SSA2} = \frac{1}{2D_{SSA}^2K_{SSA2}}. \tag{6.50}$$

Fig. 6.22 depicts the simulated step response of the 5$^{\text{th}}$ harmonic amplitude with real G_{cc2} and compares the result with the simplified model described by G_{5SSA2}. To achieve a behaviour similar to the result in fig. 6.21 ($D_{SSA} = \frac{1}{\sqrt{2}}$), the gain K_{SSA2} must be significantly lowered to

$$K_{SSA2} = \frac{1}{360}K_{SSA}. \tag{6.51}$$

Subsequently, the time constant T_{SSA2} is 360 times higher, which results in a very slowly step response as shown in fig. 6.22.
The compensation with parameters D_{cc5} and $-\varphi_{cc5}$ reduces the influence of the real G_{cc2}. As depicted in fig. 6.18, the calculated compensation current is shifted by $-\varphi_{cc5}$ and multiplied by D_{cc5}. Implementing this compensation, the behaviour can be described with eq. 6.43 again. However, this is only valid for the nominal fre-

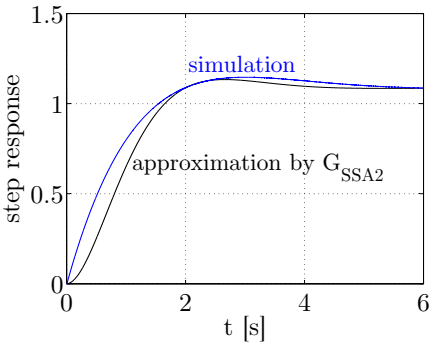


Figure 6.22: Simulation of 5$^{\text{th}}$ harmonic amplitude with real G_{cc2} and approximation by G_{SSA2}.

quency of 400 Hz. At e.g. 800 Hz,
phase shift and damping of G_{cc2} are higher. To achieve an optimized behaviour at other frequencies than 400 Hz, φ_{cc5} has to be implemented dependent on f_{pll} (calculated frequency by PLL circuit in chapter 6.6). $\varphi_{cc5}(f_{pll})$ is linearized between 400 and 800 Hz using

$$\varphi_{cc5}(f_{pll}) = \varphi_{cc5,400} + \frac{\varphi_{cc5,800} - \varphi_{cc5,400}}{400}(f_{pll} - 400). \tag{6.52}$$

where $\varphi_{cc5,400}$ is the phase shift of 5^{th} harmonic at 400 Hz (caused by G_{cc2}) and $\varphi_{cc5,800}$ is the phase shift at 800 Hz. Furthermore D_{cc5} is kept constant, since the main G_{cc2} influence is caused by the phase shift. The difference between constant and variable φ_{cc5} is shown in fig. 6.23 and fig. 6.24. The step response with constant φ_{cc5} exhibits a stable and acceptable behaviour. The G_{cc2} compensation with variable φ_{cc5} in fig. 6.24 shows better results. D_{cc5} is constant during these simulations according to eq. 6.47, i.e. the damping of G_{cc2} is compensated for only at 400 Hz. At 600 and 800 Hz the G_{cc2} damping is higher. To overcome this effect, the SSA is forced to increase the amplitude as depicted in fig. 6.23 and fig. 6.24.

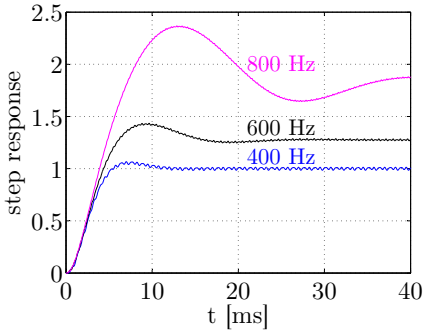


Figure 6.23: Simulated step response of 5^{th} harmonic amplitude with constant φ_{cc5} and constant D_{cc5} at different frequencies.

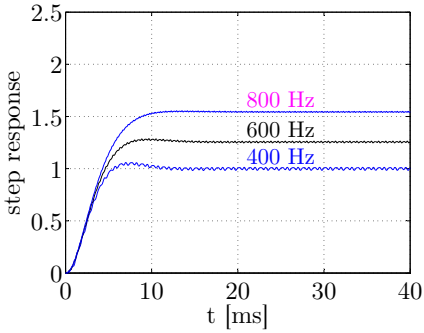


Figure 6.24: Simulated step response of 5^{th} harmonic amplitude with variable φ_{cc5} according to eq. 6.52 and constant D_{cc5}.

In the APF prototype, the SSA is implemented with variable φ_{cc5} and constant D_{cc5}.

6.6 Line synchronization with phase locked loop

To calculate the content of 5^{th} and 7^{th} harmonics, synchronization with the supply frequency is necessary. In [123], an interesting approach for real-time estimation of fundamental frequency for aerospace applications is presented. However, at least three rotating frames and a buffer for storing sampled data are required. For this application, a conventional phase locked loop (PLL) (fig. 6.25) is implemented, which is expected to require less processing power, since only one rotating frame is used and no buffer is required. The measured phase to phase voltages v_{ab}, v_{bc} and

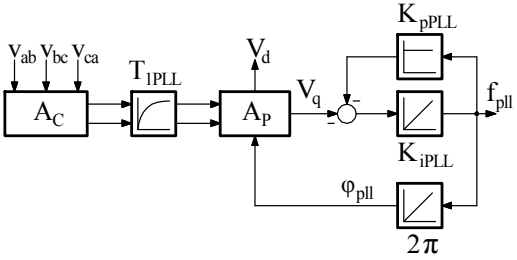


Figure 6.25: Proposed PLL circuit.

v_{ca} are transformed into the α-β-coordinate system using eq. 6.18. The transformation into the synchronous reference frame is done by

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} A_P \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \sin(\omega_{net}t) & \cos(\omega_{net}t) \\ -\cos(\omega_{net}t) & \sin(\omega_{net}t) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}. \tag{6.53}$$

The signal of interest is V_q. Considering ideal sinusoidal waveforms, V_q can be simplified to

$$V_q = 3V_{net}\sin(\varphi_e) \tag{6.54}$$

with RMS phase voltage V_{net} and phase shift between PLL and supply φ_e. The derivation of V_q is described in chapter A.1.4. The loop filter $G_{lf}(s)$ comprises an integrator with feedback K_{pPLL}:

$$G_{lf}(s) = \frac{\frac{1}{K_{pPLL}}}{1 + s\frac{1}{K_{iPLL}K_{pPLL}}} \tag{6.55}$$

Considering the phase voltage in fig. 6.7, V_q exhibits the characteristic shown in fig. 6.26. The main component is the 6^{th} harmonic with an amplitude of about 50 V. To dampen this frequency, a 1^{st} order low pass

filter with time constant T_{1PLL} is implemented:

$$T_{1PLL} = \sqrt{\frac{D_{1PLL,ref}^2 - 1}{\omega_6^2}} \tag{6.56}$$

with $\omega_6 = 6 \cdot 2\pi \cdot 360Hz$. The resulting V_q with filter is depicted in fig. 6.26.

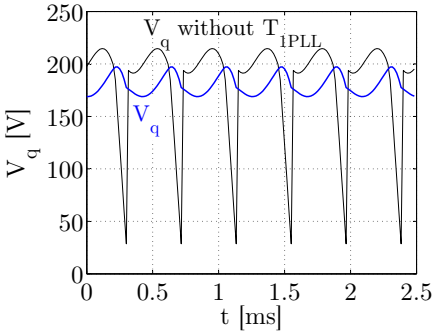


Figure 6.26: Signal V_q with and without low pass filter.

The peak-to-peak ripple is reduced by 85%. For the design of K_{pPLL}, the damping of filter T_{1PLL} at maximum supply frequency f_{max} is necessary:

$$D_{1PLL,max} = 1 + (2\pi f_{max} T_{1PLL})^2 \tag{6.57}$$

Considering this low-pass filter, the equation for V_q in steady state PLL operation ($\omega_{net} = \omega_{PLL}$) changes as follows:

$$V_q = \frac{3V_{net}\sin(\varphi_e)}{D_{1PLL,max}} \tag{6.58}$$

The calculated frequency f_{pll} is directly linked to V_q via loop filter $G_{lf}(s)$, which can be expressed in steady-state operation by

$$f_{pll} = V_q G_{lf}(0) = \frac{V_q}{K_{pPLL}}. \tag{6.59}$$

The maximum possible value for V_q appears at phase shift $\varphi_e = -\frac{\pi}{2}$. Hence, the maximum K_{pPLL} can be derived:

$$K_{pPLL,max} = \frac{3V_{net}}{D_{1PLL,max} f_{max}} \tag{6.60}$$

Considering steady state PLL operation and an occurrence of the maximum frequency step of 50 Hz, the resulting V_q has a main frequency of

50 Hz. The loop filter G_{lf} causes a phase shift of this frequency. To ensure stable tracking performance, the phase shift should be maximum $\frac{1}{4}\pi$. With these constraints, the minimal value of K_{iPLL} can be determined to

$$K_{iPLL,min} = \frac{2\pi \cdot 50Hz}{K_{pPLL} tan(\frac{1}{4}\pi)}. \tag{6.61}$$

The performance of the proposed PLL during frequency ramps and steps is described in chapter 6.7. The PLL parameters have to be optimized directly on the prototype. The presented formulas limit the parameters and offer a reasonable start value for the first experiments.

6.7 Modelling and simulation

The simulation of the APF is performed in Matlab / Simulink with toolboxes Simscape and SimPowerSystems. Fig. A.5 shows the entire model, which comprises several subsystems and C-code s-functions. All constants are defined by variables, which can be set and changed in a Matlab m-file. The analogue parts are simulated with a variable step size with a maximum of $0{,}1T_s$. The digital control parts are calculated according to the prototype settings with step sizes of T_s (basic control) and $2T_s$ (PLL + SSA). This model delivers functional and qualitative results. Power loss and EMC issues are not treated in this simulation. To keep the simulation times in an acceptable range, almost ideal components are applied. The APF inverter is modelled by a state-space average model, which allows a bidirectional power flow into the DC-link. The power supply block contains ideal frequency variable three-phase voltage sources. The source impedance is represented by L_{net} and R_{net}. All voltage and current sensors have an ideal behaviour. The diodes in the bridge rectifier have a forward voltage and differential resistance, but no reverse recovery charge. All chokes are purely inductive without capacitive or resistive parasitics. The load is a resistor with a power of P_{ECS}. The ripple filter is designed according to chapter 5.5.1. All blocks for APF control are programmed in C-code, which partly can be reused for the DSP software in the prototype.

The phase current and corresponding spectrum for the diode bridge rectifier only are depicted in fig. 6.27 and fig. 6.29. Only the 5^{th} and 7^{th} harmonics exceed the allowed limit of 2 %.

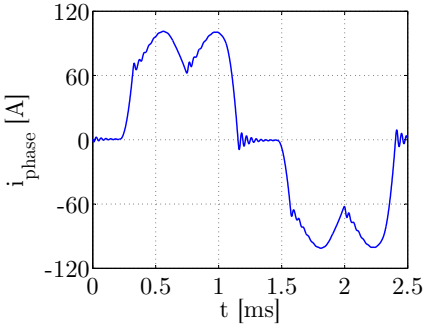


Figure 6.27: Phase current with diode bridge rectifier only (f_{net}=400 Hz)

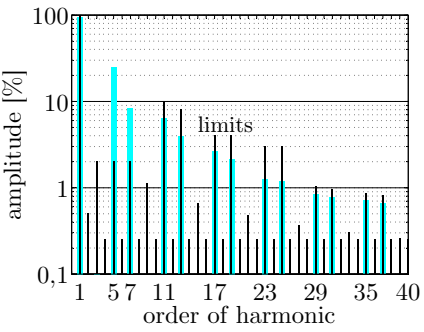


Figure 6.28: Spectrum of diode bridge current. Only the 5^{th} and 7^{th} harmonics exceed the limits.

With active power filter, the phase current changes according to fig. 6.29, the contents of 5^{th} and 7^{th} harmonics are lower than 0,1 % (fig. 6.30). The phase current and corresponding spectrum at 800 Hz are depicted in fig. 6.31 and fig. 6.32.

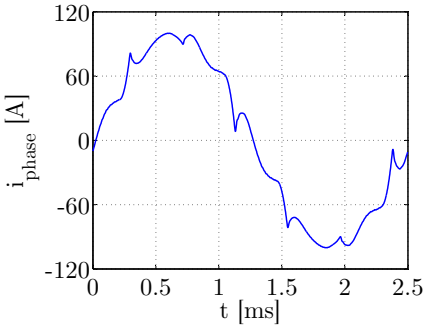


Figure 6.29: Phase current during APF operation at 400 Hz.

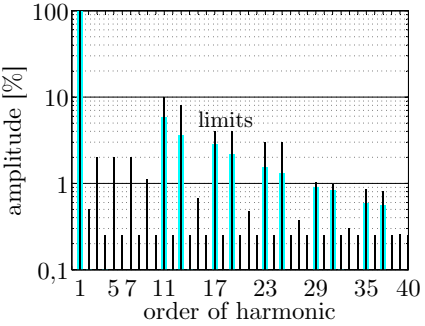


Figure 6.30: Spectrum of phase current in fig. 6.29.

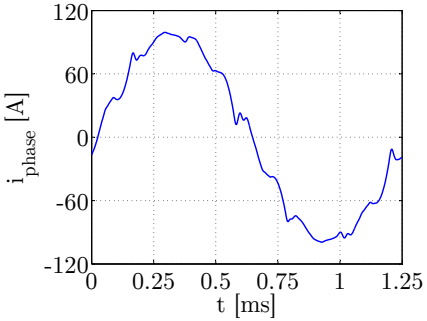


Figure 6.31: Phase current during APF operation at 800 Hz.

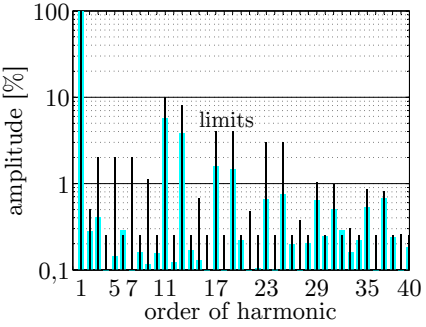


Figure 6.32: Spectrum of phase current in fig. 6.31.

The phase current change from pure rectifier to full APF operation ist depicted in fig. 6.33. The corresponding content of 5^{th} and 7^{th} harmonics is shown in fig. 6.34. After diode bridge operation during the first 10 ms, the fundamental APF control is activated, which results in about 5 A lower amplitude of the 5^{th} harmonics. The 7^{th} harmonic does not change significantly. At 22.5 ms, the selective signal analysis is activated. Now the 5^{th} and 7^{th} harmonics are compensated very accurately to amplitudes lower than 50 mA.

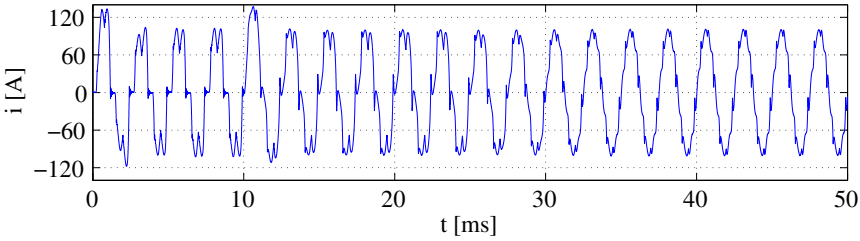


Figure 6.33: Phase current change from pure rectifier to full APF operation.

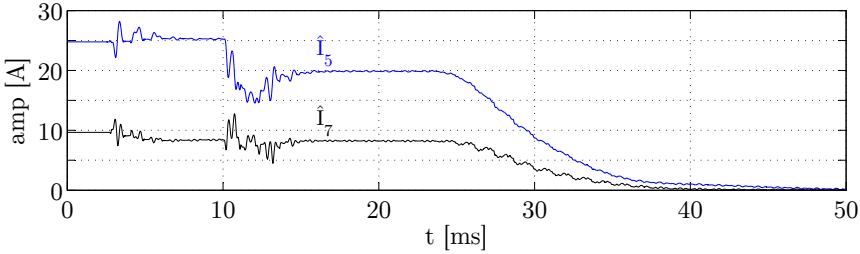


Figure 6.34: Content of 5^{th} and 7^{th} harmonics of phase current in fig. 6.33.

During APF operation, the voltage ripple at the main DC-link increases from 7.14 V to 14.63 V (fig. 6.35). As described in tab. 2.4, the DC-link must remain below 16 dBV_{RMS}, which is approximately 17.8 V_{pp}. The simulation proves the compliance with this requirement.

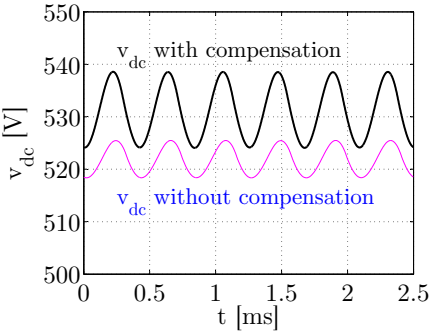


Figure 6.35: DC-link voltage of main DC-link with and without compensation through the APF.

As discussed in chapter 6.4, the voltage control cannot compensate for the power ripple caused by the compensation currents. Thus, the APF DC-

link voltage shows a ripple with a frequency of $6f_{net}$ (fig. 6.36). The peak to peak value in this working point is 33 V, which is about 3,9 % related to the mean value of 850 V. The phase current and DC-link voltage at occurrence of a load dump are depicted in fig. 6.37. The peak voltage is about 1000 V, which is slightly above the model result in chapter 6.4. This is mainly caused by the discrete simulation with 60 kHz. The steady-state condition is reached after 15 ms.

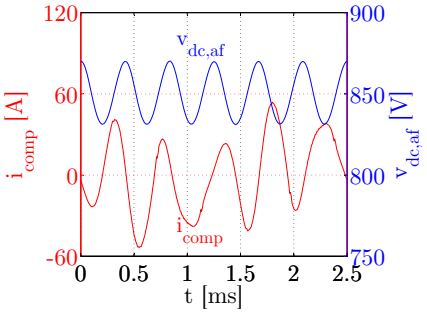


Figure 6.36: Compensation current and APF DC-link voltage during compensation.

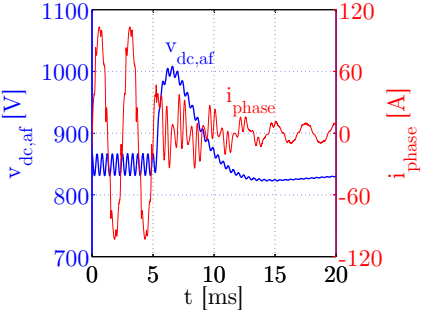


Figure 6.37: APF DC-link voltage and phase current at load dump from 46 kW to 0 kW.

The behaviour of PLL and SSA during frequency ramp and step is excellent (fig. 6.38 and fig. 6.39). There are no instabilities and the steady-state condition is achieved within 20 ms after start of the SSA (step response, fig. 6.39).

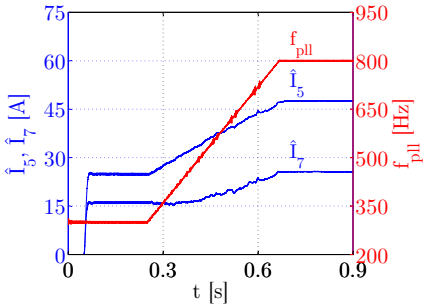


Figure 6.38: Calculated frequency and harmonic amplitudes during supply frequency ramp from 360 to 800 Hz.

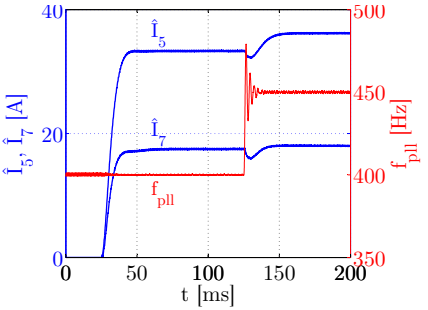


Figure 6.39: Step response of harmonics and behaviour at frequency step of supply frequency from 400 to 450 Hz.

7 Prototype and measurements

7.1 Laboratory prototype

The schematic of the laboratory prototype is depicted in fig. 5.1 and the corresponding prototype in fig. 7.2. To limit the effort of the hardware integration and manual choke production, the ripple filter is realized as single-stage LC-topology. The inverter stage (fig. 7.3) is arranged under the controller board. The numbered components are described in the following list:

1: load DC-link capacitors (each $\frac{1}{2}C_{dc}$)
2: DC-link inductors (L_{dc})
3: diode bridge rectifier and two C_y capacitors
4: filter inductors L_f
5: ripple filter with C_f and R_f
6: phase-to-phase voltage measurement
7: phase current measurement
8: EMC filter with two CM chokes, three C_x and three C_y capacitors
9: precharge circuit for APF DC-link
10: DC-link measurement
11: dual DSP controller board
12: programming interface (JTAG)
13: compensation current measurement
14: IGBT driver board
15: APF DC-link capacitors (each $\frac{1}{3}C_{dc,af}$)

In the prototype, the DC-link capacitor C_{dc} consists of two foil capacitors with each $\frac{1}{2}C_{dc}$. The APF DC-link capacitor $C_{dc,af}$ comprises three capacitors with each $\frac{1}{3}C_{dc,af}$. The load resistors are not displayed in the prototype pictures.

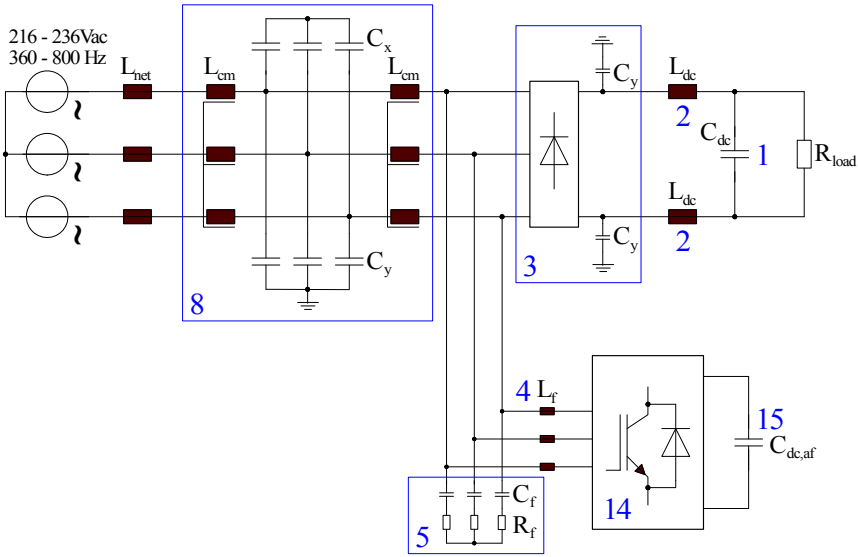


Figure 7.1: Schematic of laboratory APF prototype.

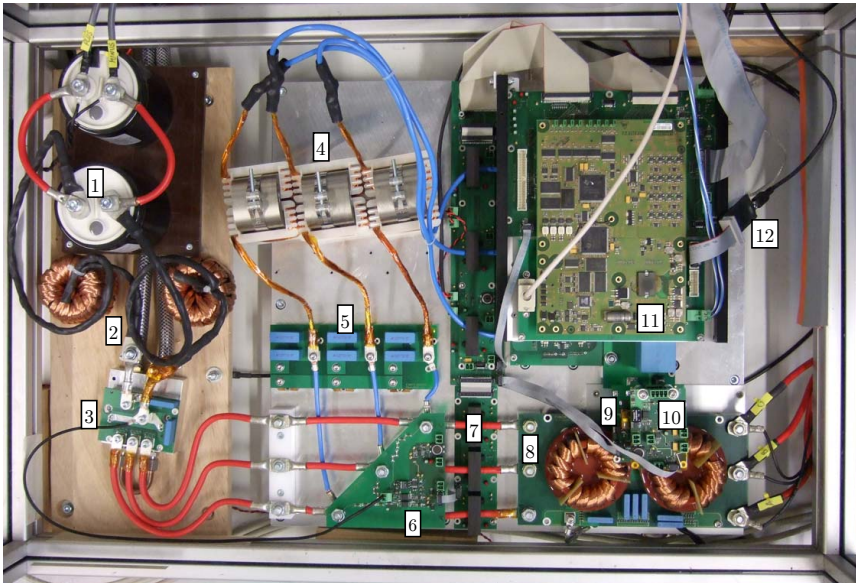


Figure 7.2: Laboratory APF prototype.

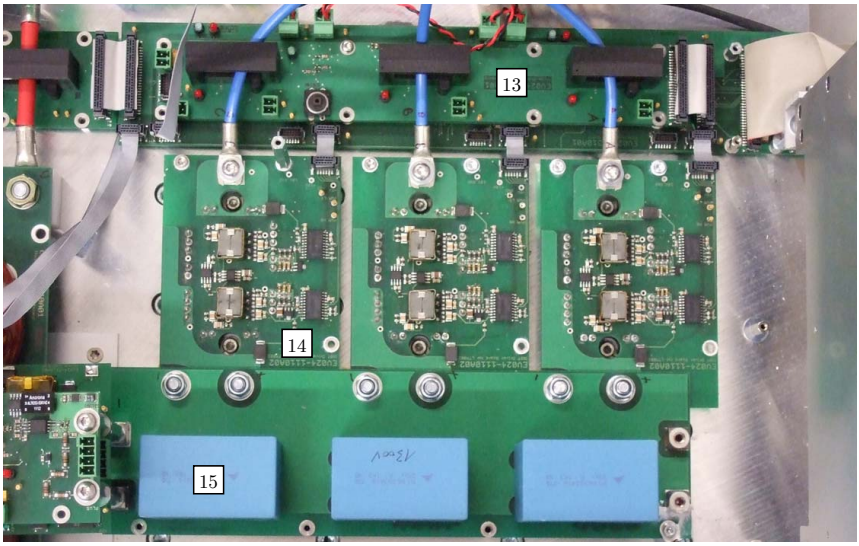


Figure 7.3: Power stage with three SP3-modules.

7.2 Software implementation in Dual-DSP board

The implementation of the proposed control architecture in one state-of-the-art digital signal processor (DSP) is not possible, since the processing power is not sufficient. That is why the control algorithm is distributed into two DSPs (fig. 7.4), which are linked by multi channel buffered serial port (McBSP). The proposed task scheduling of DSP 1 and DSP 2

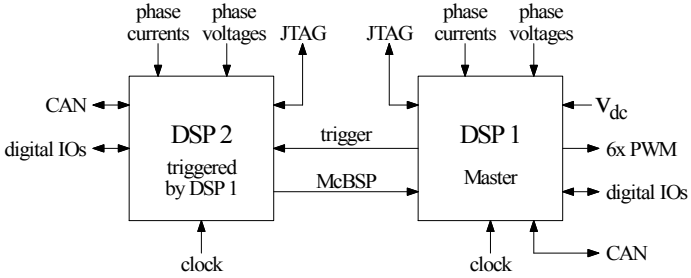


Figure 7.4: Schematic of DSP controller board.

is depicted in fig. 7.5. DSP 1 calculates the instantaneous power and performs current control and DC-link voltage control (task 1). DSP 2 calculates PLL and selective signal analysis (task 2). DSP 1 is triggered by

the PWM frequency of 60 kHz, DSP 2 is triggered by DSP 1 with half the PWM frequency (30 kHz). The low priority CAN communication and

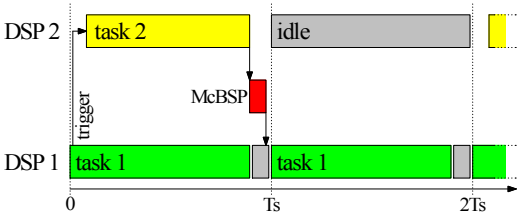


Figure 7.5: Task scheduling of DSP 1 and DSP 2.

digital IO processing are performed in idle phases. After calculation of PLL and SSA, three current values $i_{ref,SSA}$ are sent to DSP 1. The input buffer of the McBSP interface has a size of only 32 bit. A transfer of e.g. three float32 variables would mean that DSP 1 has to read and clear the input buffer after receiving the first number. Then, DSP 1 would allow the transfer of the next float32 number and so on. During the entire transfer process DSP 1 would be blocked and could not perform other calculations. Considering a McBSP clock of 37.5 MHz, the transfer of 32 bit data requires 853 ns without overhead. DSP 1 would lose several µs of calculation time. That is why the three currents $i_{ref,SSA}$ are compressed into one float32 variable (each ±9 bit fixed-point). This avoids interaction between the two DSPs, since no data flow control is necessary. The phase voltages and phase currents are sampled by both DSPs and are not transferred via McBSP, since the time required for analogue-digital conversion (ADC) of analogue signals is significantly shorter. The communication via controller area network (CAN) is used for remote control and analysis of signals using a laptop.

The DSP code consists of several C-code s-functions, which are connected in the Matlab / Simulink environment. The entire program is consolidated via autocode generation and flashed with Code Composer Studio from Texas Instruments. To achieve the required calculation time of less than 16 µs, some measures have to be implemented:

- application of C-code s-functions to avoid inefficient autocode; autocode generation only connects the different s-functions
- complete program runs in random-access memory (RAM), not in flash memory
- sine and cosine operations use look-up tables
- no use of square roots
- minimization of divisions by conversion to multiplications and multiuse of intermediate results

- use of as few as possible function calls to reduce stack operations
- use of 16 bit integer and 32 bit float numbers, no 64 bit double numbers
- polling instead of interrupts
- optimized ADC configuration for fast sampling
- ADC is faster than McBSP communication ⇒ sampling of phase currents and phase voltages by both DSPs
- reduction of McBSP communication time by data compression

The long communication time and the small input buffer represent a disadvantage of the McBSP communication. A better solution is the connection of the two internal DSP buses using a parallel 16 bit or 32 bit interface, which results in very short communication times using direct memory access (DMA). However, the best controller topology for this application is a combination of field programmable gate array (FPGA) and DSP. The FPGA performs the complete control algorithm and the DSP is responsible for management and CAN communication.

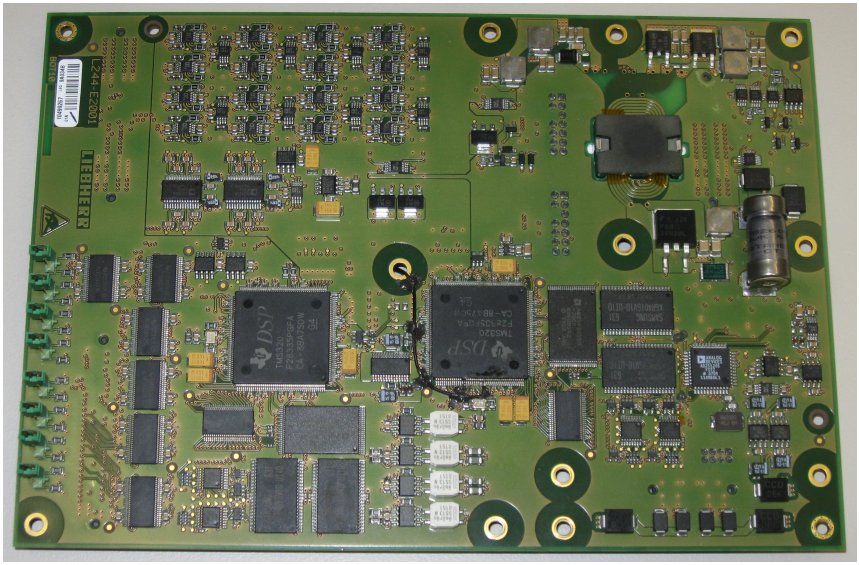


Figure 7.6: Dual-DSP board with two 28F335 motion control DSPs from Texas Instruments. The DSP internal flash and RAM is extended by additional memory chips.

7.3 Compensation performance under steady state and transient conditions

Up to about 110 V phase voltage and 400 V in the APF DC-link, the APF operation is stable under all conditions. With higher voltages and at supply frequencies above 600 Hz, the APF control causes an overcurrent at start-up. The hardware safety function interrupts the PWM signals automatically and the APF operation is stopped. The overcurrent is a consequence of the small filter inductance L_f. The resulting time constant and gain K_{cc} are too small for the 60 kHz current control loop. To continue the further evaluation of control algorithm, the filter chokes are replaced by new ones with a four times higher inductance. The following measurement results are all performed with these modified chokes at 130 V phase voltage, 600 V APF DC-link voltage and load resistor of 5.39 Ω, which results in an output power of about 16 kW. The input filter (LCL-topology) and ripple filter (LC-topology) are implemented as shown in fig. 5.1.
All steady-state harmonics measurements are performed with a power analyzer LMG500 from ZES Zimmer (chapter A.3.1), which offers a significantly higher sampling accuracy than standard oscilloscopes. The corresponding spectra are derived by analysis of the sampled phase currents in Matlab. 10 periods in time domain are used for the harmonics calculation. The presented results are the mean value of the three analyzed phases.
The phase currents during steady state compensation at 400 Hz and 800 Hz are depicted in fig. 7.7 and fig. 7.9, respectively. The corresponding spectra in fig. 7.8 and fig. 7.10 prove the compensation quality. The 5^{th} and 7^{th} harmonics are reduced to less than 0,2 %. However, some low frequency even harmonics exceed the limits. Possible reasons are inverter asymmetries, sensor non-linearities and sideband effects due to the non-linear PWM with discrete resolution. This topic has to be further investigated in detail.
At 800 Hz, the 29^{th} and 31^{th} harmonic exceed the limits. This effect is caused by the rectifier commutation as described in chapter 5.5.1. Since the prototype has a LC ripple filter with 1 Ω damping resistor, the resonant circuit with L_{net}, C_f and C_{xy} is stimulated by the commutation and causes a ringing with frequency

$$f_{ring} = \frac{1}{2\pi\sqrt{L_{net}\left(C_f + C_{xy}\right)}}. \tag{7.1}$$

With $L_{net} = 56\mu H$ (eq. 2.1), $C_f = 660nF$ (eq. 5.40) and $C_x = C_y = 30nF$ (eq. 5.43), the resulting ringing has a frequency of about 25 kHz, which is in the range of the 31th harmonic at 800 Hz.

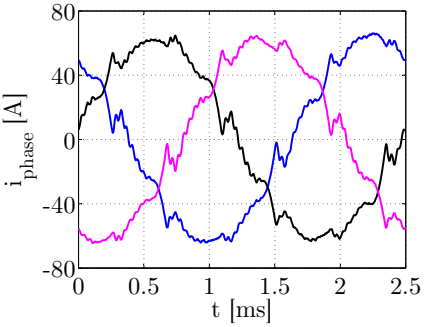


Figure 7.7: Measured phase currents (f_{net}=400 Hz, V_{net}=130 V).

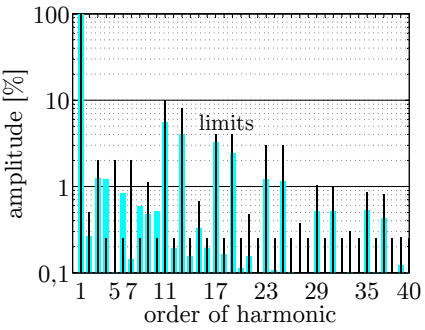


Figure 7.8: Harmonics of phase currents at 400 Hz (mean value).

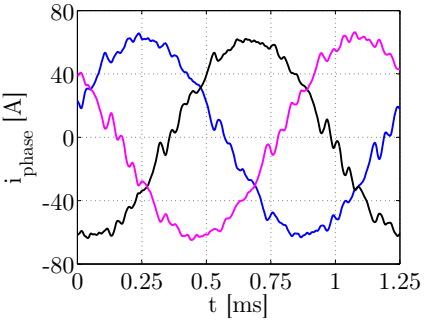


Figure 7.9: Measured phase currents (f_{net}=800 Hz, V_{net}=130 V).

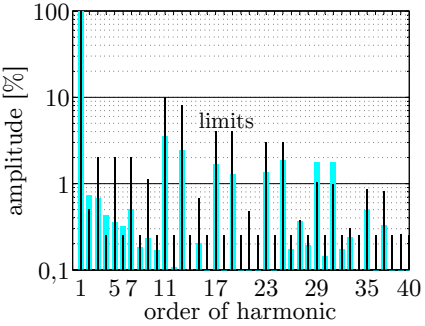


Figure 7.10: Harmonics of phase currents at 800 Hz (mean value).

The behaviour of 5th and 7th harmonics amplitudes after activation is displayed in fig. 7.11. The steady-state condition is reached after about 200 ms. The amplitudes during frequency ramp and step are depicted in fig. 7.12 and fig. 7.13. The compensation is stable at any time. The calculated frequency (fig. 7.14) has a maximum ripple of ±10 Hz. By reducing the gain of the SSA, the gain of the PLL can be reduced, too, which results in lower frequency ripple. As shown in fig. 7.8, the steady-state phase current quality is excellent and therefore a PLL optimization is not necessary.

As described in tab. 2.1, the supply phase voltages may have a total harmonic distortion (THD) of 10 % and an asymmetry of +3 V_{RMS} between two phases. The device must continue its operation without instabilities

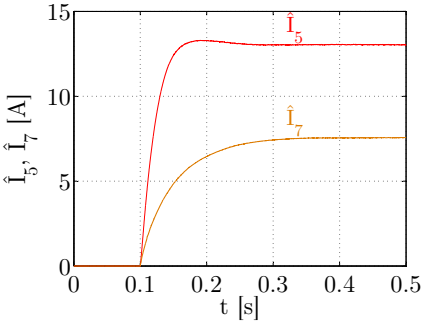


Figure 7.11: Behaviour of harmonic amplitudes after start-up (step response).

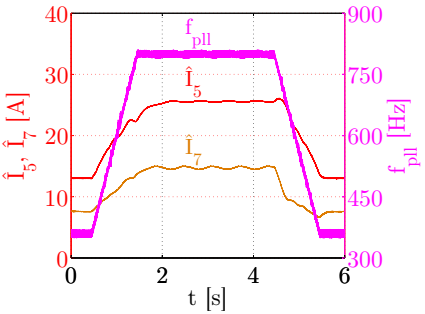


Figure 7.12: Measured behaviour of implemented PLL and calculated amplitudes of 5th and 7th harmonics during ramp of 440 Hz/s.

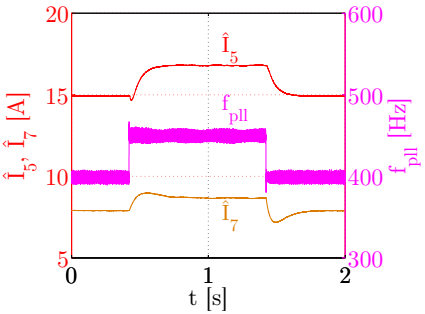


Figure 7.13: Behaviour of f_{PLL}, 5th and 7th harmonics during step of 50 Hz/ms.

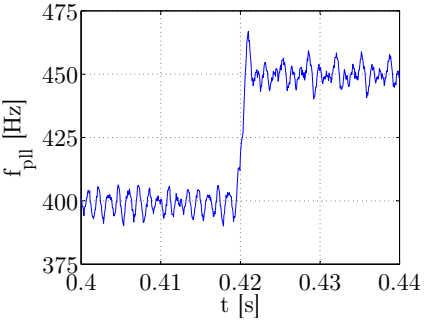


Figure 7.14: Magnified diagram of f_{PLL} during frequency step.

and damage. The harmonics compliance is not required during these two modes of operation. The distortion using a triangular supply voltage has a THD of 16 %, which is significantly above the required 10 % (fig. 7.15). The compensation quality is nearly identical to the result in fig. 7.7. During asymmetric amplitudes of the supply voltage, the phase currents show different amplitudes, but the stability is not reduced (fig. 7.16).

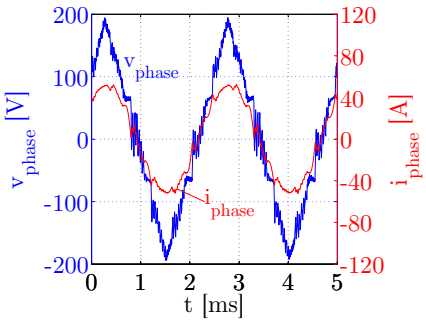


Figure 7.15: Triangular supply phase voltage and phase current during compensation.

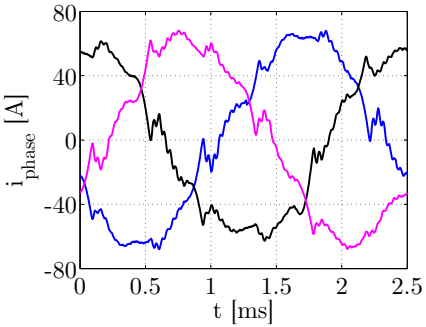


Figure 7.16: Phase currents during compensation with asymmetric phase voltage amplitudes.

7.4 Robustness under failure conditions

A transient overvoltage[1] (fig. 7.17) and phase loss of one or all phases (fig. 7.19 and fig. 7.21) are operation conditions, where the APF cannot continue its operation. In these cases, the APF must be deactivated rapidly without any damages or critical overcurrents by control instabilities. In this prototype, a hardware circuit for over- and undervoltage of the three input phases is integrated. This function switches off the APF independently from the control software in case of a failure. The resulting phase currents for transient overvoltage and loss of one or all phases are depicted in fig. 7.18, fig. 7.20 and fig. 7.22. In all diagrams, the sampling of all signals is triggered by the fault signal, which switches off the APF at t=0 ms. The detection of failure needs maximum 100 µs, depending on the type of failure. High currents after deactivation of the APF at t>0 are inrush currents (overvoltage) and charging currents of the main DC-link (phase loss). These experiments demonstrate the robustness of the active power filter, since there are no control instabilities or critical overcurrents caused by the APF.

The most critical failure case for the APF is a full load dump. Here, the APF DC-link is charged rapidly, which could lead to a critical overvoltage. The performance of the implemented PID-controller for the APF DC-link voltage is shown in fig. 7.23. During a full load dump from 17 to 0 kW, the overvoltage can be limited to 115 % of the nominal value. This is not

[1] Tab. 2.1 defines an overvoltage of 360 V_{RMS} at 230 V_{RMS} steady-state voltage. This is factor 1.56. In this experiment, the steady-state voltage is 130 V_{RMS} and therefore the overvoltage is 203 V_{RMS}.

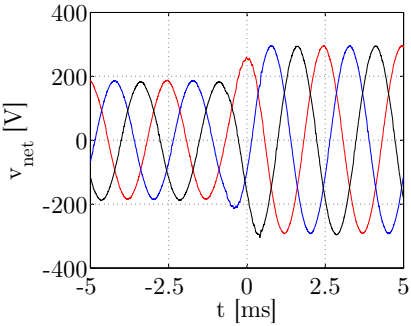


Figure 7.17: Input phase voltages (before source inductance) for transient overvoltage.

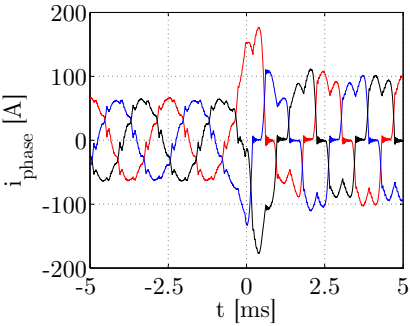


Figure 7.18: Input phase currents at transient overvoltage.

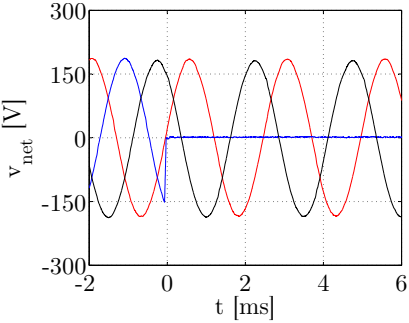


Figure 7.19: Input phase voltages (before source inductance) for loss of one phase.

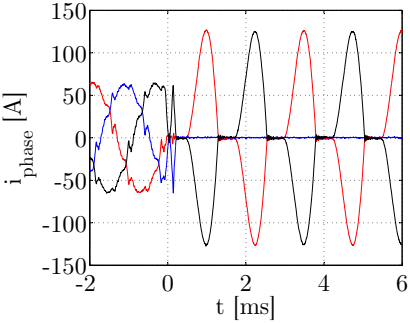


Figure 7.20: Input phase currents at loss of one phase.

critical for the DC-link capacitor. Since the SSA has a time constant of about 150 ms, the injection of harmonics continues after the load dump. This is not critical for the voltage control, since the harmonics exchange AC power only and do not have an influence on the mean voltage.

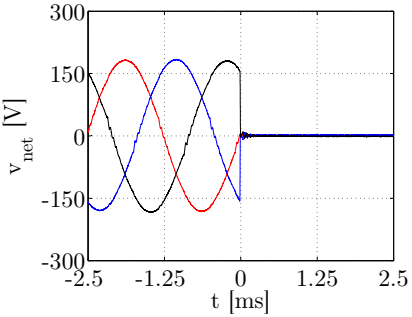


Figure 7.21: Input phase voltages (before source inductance) at loss of all phases.

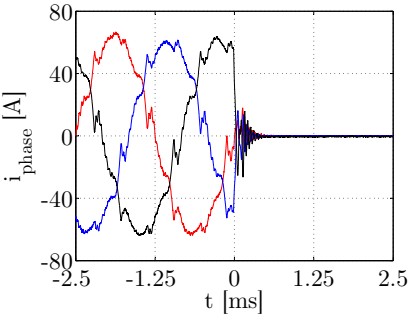


Figure 7.22: Input phase currents at loss of all phases.

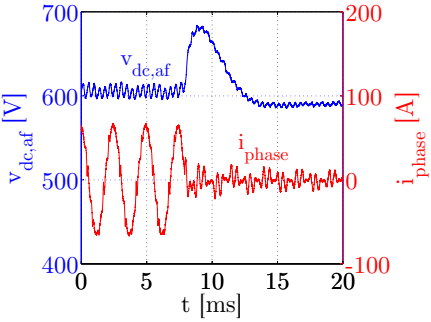


Figure 7.23: APF DC-link voltage at load dump.

7.5 Validation of power losses and temperatures

The power is measured at different points with the LMG500, a power analyzer with four current and four voltage channels (chapter A.3.1). Fig. 7.24 shows an overview of the prototype and the location of current and voltage sensors for the measurement of total input power P_{in} and total load power P_{load}. With the gathered information, the overall power loss and efficiency can be determined. For measurement of P_{in2} and P_{APF}, the location of LMG500 voltage and current sensors must be changed. All results of the performed measurements are summarized in tab. 7.1.

The total power loss of the APF only (P_{APF}) is directly measured via phase voltage and i_{comp} (fig. 7.25) at the APF connection point. P_{APF} comprises

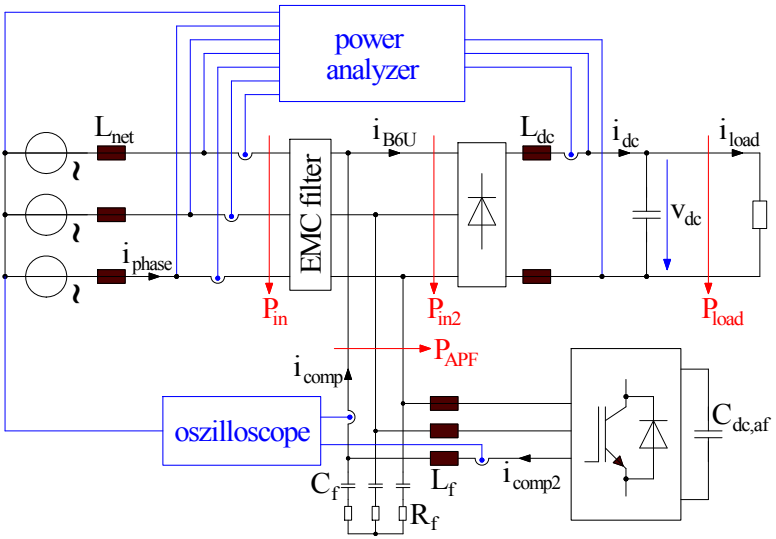


Figure 7.24: Measurement of total input power P_{in} and load power P_{load}. For measurement of P_{in2} and P_{APF}, the location of LMG500 voltage and current sensors must be changed.

the inverter power loss ($P_{APF,inv}$), total power loss in all inductors L_f (P_{Lf}) and damping power loss of all resistors R_f (P_{Rf}). The power losses in DC-link capacitor $C_{dc,af}$ and filter capacitor C_f are not taken into account. To derive the loss of the damping resistors R_f, the compensation current before (i_{comp2}) and after the ripple filter (i_{comp}) are measured using an oszilloscope. The difference between these two currents is the damping current through R_f. For the power loss in L_f, the spectrum of i_{comp2} and the resistance of L_f vs. frequency are necessary (fig. 7.26). By summing up the losses at every single frequency, the total copper power loss in L_f can be determined. The magnetic power loss is not taken into account.

The total power loss in the two DC-link inductors L_{dc} (P_{Ldc}) is calculated using the DC-resistance of L_{dc} and the RMS value of i_{load}. The dominant component is the DC current and hence the higher harmonics are not taken into account as done with L_f. The rectifier power loss P_{B6U} is then

$$P_{B6U} = P_{in2} - P_{load} - P_{Ldc}. \tag{7.2}$$

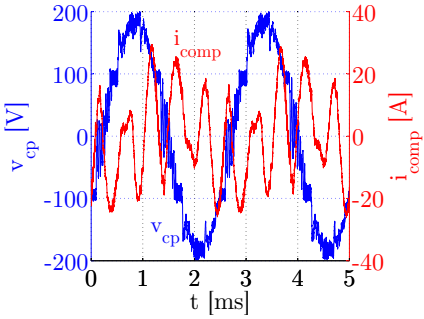


Figure 7.25: Voltage and compensation current of phase A at APF connection point.

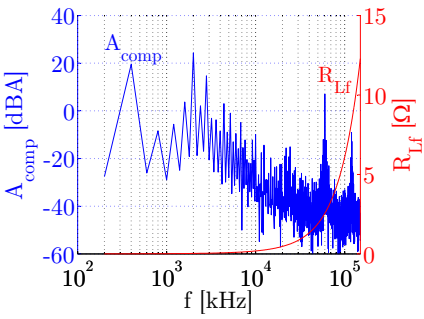


Figure 7.26: Spectrum of compensation current and ohmic resistance of L_f vs. frequency.

The power loss in the input filter is determined by

$$P_{IF} = P_{in} - P_{in2} - P_{APF}. \tag{7.3}$$

The input filter has a total ohmic resistance of 2,1 mΩ per phase. This is measured by the voltage drop at a test current of 100 A_{dc}. Considering a phase current of 44 A_{RMS}, the total input filter power loss is about 12 W. Hence, the calculated values in tab. 7.1 are in the correct range. Deviations to the calculated 12 W are caused by measurement uncertainties. For frequencies between 65 Hz and 3 kHz, the power analyzer LMG500 has a power measurement uncertainty of ±0,028% of the measured value plus ±0,03% of the measurement range (fig. A.7). During APF operation with NPT-IGBTs, the total input power is 17225 W, i.e. one phase delivers 5472 W. The LMG500 voltage range is 250 V and the current range 60 A[2] (fig. A.6). This corresponds to a power range of 15 kW. The corresponding measurement uncertainty per phase is

$$P_{err} = \pm\big(0{,}00028 \cdot 5472W + 0{,}0003 \cdot 15kW\big) \approx \pm 6\ W. \tag{7.4}$$

The uncertainty of the total input power loss is then ±18 W.

The calculation with the measured compensation current and an APF DC-link voltage of 600 V yields losses of 605 W for the APF inverter with NPT-IGBTs and 199 W for the SiC version. Tab. 7.2 compares the

[2]External current transducers [124] with a ratio of 1000:1 are used during all measurements. The resulting LMG500 internal measurement range for the phase current measurement is 60 mA. Together with the ratio of 1000:1 the relevant range is 60 A.

	rectifier only	**APF with IGBTs**	**APF with MOSFETs**
Input			
P_{in} [W]	**15823**	**17225**	**17037**
S_{in} [VA]	16815	17399	17227
P_{IF} [W]	8,8	14,2	25,6
V_{phase} [V_{RMS}]	129	130	130
I_{phase} [A_{RMS}]	43,5	44,5	44,1
APF			
P_{APF} [W]	0	550	297
P_{Rf} [W]	0	11,9	13,0
P_{Lf} [W]	0	41,0	46,8
$P_{APF,inv}$	0	**497**	**237**
I_{comp} [A_{RMS}]	0	14,2	14,9
Rectifier			
P_{in2} [W]	**15814**	**16661**	**16715**
P_{B6U} [W]	153	163	162
I_{B6U} [A_{RMS}]	43,4	45,2	44,8
Load			
P_{load} [W]	**15632**	**16467**	**16522**
V_{dc} [V_{RMS}]	290	298	297
I_{load} [A_{RMS}]	53,8	55,4	55,6
P_{Ldc}	29,0	30,6	30,9
Overall figures			
P_{tot} [W]	191	758	516
efficiency [%]	98,8	95,6	97,0
cosφ	0,941	0,990	0,989

Table 7.1: Results of loss measurements and relevant parameters. Directly measured power values are set bold.

calculated and measured power loss results. The APF inverter with NPT-IGBTs has 18% lower power loss than calculated. This is due to the used worst case values, which are higher than the values of the characterization. The power loss of SiC-MOSFET inverter is 19% higher. One reason for the higher power loss could be high manufacturing tolerances, since the used SiC-chips are only engineering samples. Another reason could be the

calculated power loss of L_f. Since the magnetic power loss is not considered, the calculated 46,8 W could be too low. A third reason could be the higher dv/dt of the SiC-inverter, which results in a higher disturbance of the power analyzer. The experience shows that power measurements with switched voltages at inverter outputs are generally not very accurate.

	calculated power loss [W]	**measured power loss [W]**	Δ [%]
NPT-IGBT module	605	497	-18%
SiC-MOSFET module	199	237	+19%

Table 7.2: Comparison of calculated and measured power loss of APF inverter.

The calculated junction temperatures at full power are shown in tab. 7.3. Considering the cooling plate surface temperature of 89 °C, the IGBT chip has a ΔT of 45 K and the MOSFET of 23 K. To take into account the difference to the measurement, these values are multiplied with 0,82 (-18%) and 1,19 (+19%). The resulting predicted junction temperatures at full power are 126 °C (IGBT) and 117 °C (MOSFET, tab. 7.3). Both values are not critical, since the rated junction temperatures are 150 °C (IGBT) and 175 °C (MOSFET). However, it is necessary to repeat this measurement at full power to verify the predicted junction temperatures. If possible, the junction temperatures should be directly monitored during operation by an infrared camera. Alternatively, the $V_{ce}(t)$-method may be applied. For this technique, the APF inverter runs in normal operation until the steady-state temperatures are reached. After switching off the APF inverter, the V_{ce} voltage drop for a defined test current enables a determination of junction temperature.

	calculated T_J [°C]	**predicted T_J [°C]**	Δ [%]
NPT-IGBT	134	126	-6,0%
SiC-MOSFET	112	117	+4,5%

Table 7.3: Comparison of calculated and predicted junction temperatures at full power of 46 kW.

7.6 EMC measurements

The DM and CM disturbances are measured with an EMI receiver from Rohde & Schwarz. The power supply neutral is connected to earth during all EMC measurements. APF prototype is mounted on an aluminium plate, which is connected to earth, too. The DM voltage is measured directly at the inverter output with respect to neutral (fig. 7.27). The resulting DM currents (fig. 7.28) in the input phases of the supply are measured with the power analyzer until 150 kHz (with source inductance) and by the EMI receiver for frequencies above 150 kHz (with LISN). As predicted by the calculation in chapter 5.5.1, the emitted disturbance exceeds the limit. At least a two-stage ripple filter is necessary to significantly lower the DM currents.
The CM voltage is measured at the APF DC-link minus rail with respect to neutral (fig. 7.29). The resulting CM current at the input phases (fig. 7.30) slightly exceeds the allowed limit. This is quite near the calculation result of chapter 5.5.2, which predicts a scarce compliance of CM currents. To lower the CM emission, a higher value for the CM chokes is necessary.

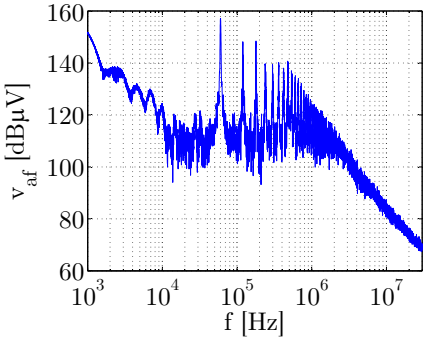


Figure 7.27: Differential output voltage of APF inverter.

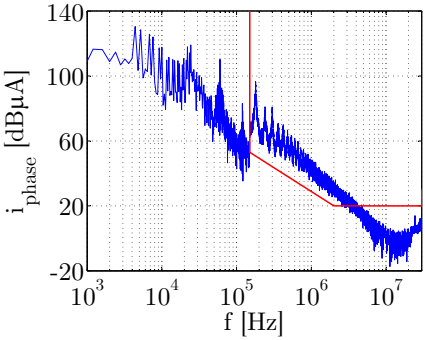


Figure 7.28: Differential current spectrum of one input phase.

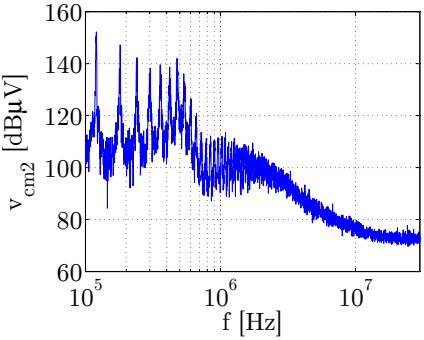


Figure 7.29: Common-mode voltage spectrum of APF DC-link.

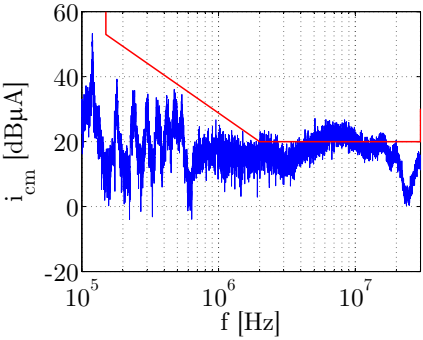


Figure 7.30: Common-mode current spectrum at three-phase input.

7.7 Evaluation of active power filter

The active power filter is the most flexible topology, since it is able to compensate for the harmonics of several devices. The connection point in the electrical grid is variable and therefore the APF is suited for retrofit programs of existing airplanes. The APF is designed for 40 % of the total phase current only, which results in lower weight than for ATRU and APFC.

In contrast to the APFC, only the power modules and APF DC-link see a CM voltage and therefore the CM currents are lower. However, the differential currents are more critical, since the ripple filter must take into account the ringing with the source inductance. This ringing is caused by the rectifier commutation and has to be reduced by damping and improved ripple filter topologies. Another disadvantage of the APF is the complex control algorithm, which has to be calculated within 16 µs. The necessary processing power requires two DSPs or a DSP-FPGA combination, which leads to high development and qualification costs. The measurements demonstrate that the critical operation modes

DC-link chokes	0,20
filter inductors	0,19
input and ripple filter	0,14
controller board and sensors	0,05
power modules and driver boards	0,05
DC-link board and capacitors	0,04
rectifier and PCB	0,01
sum	**0,68**

Table 7.4: Weight distribution of complete APF, normalized to ATRU weight.

are mastered excellently. The APF exhibits a high ruggedness against supply frequency variations, asymmetric and distorted supply voltage and load dump. The compensation of 5^{th} and 7^{th} harmonic is superior, but the generation of low frequency even harmonics is still an open topic, which has to be investigated in detail. The EMC targets could not be fulfilled by the prototype. Both CM and DM measurements show that the input and ripple filter design is not yet optimized. However, the EMC calculations predicted both the significant DM non-compliance and the scarce CM non-compliance.
The weight distribution of complete APF[3] is summarized in tab. 7.4. The biggest portion cause the DC-link and filter chokes. The use of the APF does not require output CM chokes at the main inverter output, since the CM voltage swing of the load DC-link is significantly lower compared to the APFC.

[3]The presented weight distribution is not valid for the shown laboratory prototype. It is valid for the final APF, which will be integrated in a series device.

8 Summary

In order to contribute to weight reduction concerning the MEA, this work investigates the combination of 6-pulse diode rectifier with an active power filter (APF) as an alternative to the conventional rectifiers autotransformer rectifier unit (ATRU) and active power factor correction (APFC). The use of a diode bridge rectifier alone is not possible due to the high current harmonics. Next to the housing, the rectifier causes the biggest portion of weight and hence offers a large potential for weight savings. The APF compensates for the 5^{th} and 7^{th} harmonics only and therefore must be designed for 40% of the entire phase current only. The conventional topologies must be designed for the full phase current. This advantage reduces the total rectifier weight.

The power module for the APF has to be chosen carefully, especially with respect to the power loss. At the maximum supply frequency of 800 Hz, the 7^{th} harmonic has a frequency of 5.6 kHz. To ensure at least factor 10 between switching and APF output frequency, the switching frequency is set to 60 kHz. The most promising semiconductor module comprises 1700 V SiC-MOSFETs with 1700 V SiC free-wheeling diodes. The determination of E_{on}, E_{off} und E_{rr} is done using the common double-pulse test. The conduction properties are derived by a curve tracer and the thermal characteristic is measured using the $V_{ce}(T)$-method. The magnitudes of 5^{th} and 7^{th} harmonics for the analytic loss calculation are determined by simulation. The total power loss in the SiC-MOSFET module is about 26% of the used benchmark module with NPT-IGBTs. The electrical characterization shows that the parasitic inductances of the conventional module technology are too high for the application of SiC-MOSFETs. The high switching speed requires more compact modules with optimized connection to the DC-link capacitance.

The calculation of EMC-filter is done using the quadripole theory, which divides a complex network into four-element matrices. These matrices can be processed and analyzed e.g. in a Matlab environment. One result is that the common-mode emissions of the APF are lower than for the APFC, since the parasitic capacitances against earth of the floating parts are significantly smaller. The design of ripple filter, which damps the switched

voltage of the APF inverter, must consider the subsequent resonant circuit with the source inductance. This circuit is stimulated by the rectifier commutation and therefore must be additionally damped. The resulting damping resistors reduce the filter performance especially at frequencies above 100 kHz. That is why a two-stage ripple filter is necessary to achieve sufficient damping at higher frequencies. The filter design and emissions are determined mathematically and validated in the laboratory setup.

Another main task, next to the design of the APF hardware, is the analysis and design of the control algorithm. The coupling impedance between APF and supply net is very small taking into account the maximum allowed DC-link voltage of 900 V. To ensure stability, the current control gain must be configured moderately. The resulting compensation quality is not sufficient due to the high systematic error with the P-control and small allowable gain. That is why the selective harmonic compensation is introduced as additional control stage. The combination of fast basic control with PLL-less reference current generation based on instantaneous power theory and slower but precise harmonic selective compensation represents a new control concept, which meets all dynamic and static requirements. An appropriate patent has been submitted in the frame of this work ([125], [126], [127]). Furthermore the robustness is higher, since a failure of the selective analysis does not affect the basic control and thus a minimal compensation is guaranteed. This novel safety concept is supported by the choice of controller architecture with two equivalent digital signal processors (DSP). DSP 1 performs the basis control and takes care of the DC-link voltage. DSP 2 synchronizes itself with the three-phase supply via PLL and analyses the content of 5^{th} and 7^{th} harmonics. If DSP 2 fails or the PLL loses synchronization, a compensation with lower quality is still maintained. The design of the control algorithm is analysed and simulated comprehensively by means of Matlab and Simulink before running the prototype in the laboratory.

The design of the APF-hardware is validated by measurements. During static compensation the amplitudes of 5^{th} and 7^{th} harmonics are reduced to less than 0.1%. A high distortion of supply voltage by using a triangle phase voltage does not have an influence on the compensation quality. Differences in phase voltage amplitudes do not affect the APF operation. The dynamic performance during frequency step and ramp of the phase voltages is superior. The APF follows the supply voltage without any instabilities or failures. By adequate configuration of the DC-link voltage control, the short-term overvoltage at full load dump is limited to 115% of the steady-state DC-link voltage. During abnormal events such as sup-

ply overvoltage and phase loss of one or all phases, the APF switches off immediately to prevent high destructive currents. The measurements confirm the compliance of the proposed APF with the corresponding standard RTCA DO160.

To conclude, this work proves the functionality of an active power filter at a three-phase supply with variable frequency of up to 800 Hz. With this topology, the weight of the rectifier is reduced by 33% compared to a conventional autotransformer unit. The power density of the complete power electronic device increases by 20%. The novel two-stage control structure sovereignly fulfils all static and dynamic requirements. This concept is supported by the chosen dual-DSP controller architecture. The topic of wide-band-gap power semiconductor devices is also taken into account by using SiC-MOSFETs and SiC-diodes in the APF inverter stage. This is necessary due to the high switching frequency of 60 kHz.

The results of this work motivate the implementation of the proposed new rectifier topology for the More Electric Aircraft (MEA). The biggest advantage of the APF is the modularity and flexibility, which allows the use with several power electronic devices. In this configuration, the APF offers the greatest weight savings.

The next step is the increase of switching frequency to lower the weight of the ripple filter inductors. However, the existing DSPs must be replaced by new ones with more processing power. Furthermore, the current sensing technology will be optimized by using Δ-Σ-converters, which do not require pulse-mid sampling. This measure will result in a higher sampling quality and enables the use of a higher current control gain, which reduces the systematic control error and increases the control stability. The mentioned optimizations could be subject of future works.

A Appendix

A.1 Derivation of equations

A.1.1 Derivation of eq. 3.27

The current through a rectifier diode in the APFC circuit (fig. 3.25) is shown in fig. A.1. The E_{rr} of a diode is strongly dependent on the current, which flows directly before the diode blocks. The duty cycle is not taken into account. The total characteristic in fig. A.1 is divided into six areas. Area A is defined as follows:

$$A = \left(\hat{I}_{phase} - \frac{1}{2} I_{PP}\right) \int_{0}^{\frac{T}{6}} sin(\omega t) = \frac{1}{2\omega}\left(\hat{I}_{phase} - \frac{1}{2} I_{PP}\right) \tag{A.1}$$

with phase current amplitude $\hat{I}_{phase}$, peak-to-peak ripple current I_{PP}, $\omega = 2\pi f_{net}$ and $T = \frac{1}{f_{net}}$. Area B is defined as follows:

$$B = \frac{1}{2}\left(\hat{I}_{phase} - \frac{1}{2} I_{PP}\right) \int_{\frac{1}{12}T}^{\frac{1}{6}T} sin(\omega t) = \frac{1}{4\omega}\left(\hat{I}_{phase} - \frac{1}{2} I_{PP}\right)\left(\sqrt{3} - 1\right) \tag{A.2}$$

Area C has approximately the same size as area B. The mean current $\hat{I}_{Dr,sw}$ can then be defined:

$$\hat{I}_{Dr,sw} = \frac{1}{T}\left(2A + 4B\right) = \frac{\sqrt{3}}{2\pi}\left(\hat{I}_{phase} - \frac{1}{2} I_{PP}\right) \tag{A.3}$$

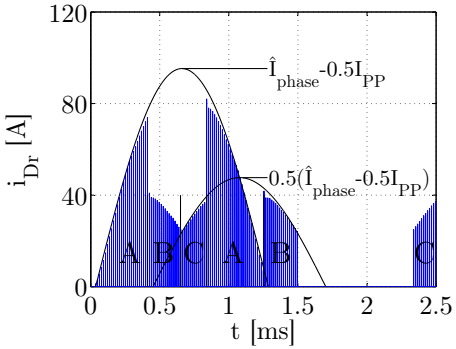


Figure A.1: Current through rectifier diode over one period (f_{net}=400 Hz).

A.1.2 Derivation of eq. 5.9

The APF injects harmonics into the main supply, which leads to an AC power flow delivered by the APF DC-link. The resulting voltage ripple at the DC-link has a frequency of $6f_{net}$, the amplitude is dependent on the size of $C_{dc,af}$.For the following calculations, the phase voltages are assumed to be purely sinusoidal. They are calculated using

$$v_a(t) = \sqrt{2}V_{net}sin(\omega_{net}t), \tag{A.4}$$

$$v_b(t) = \sqrt{2}V_{net}sin\left(\omega_{net}t + \frac{2}{3}\pi\right), \tag{A.5}$$

$$v_c(t) = \sqrt{2}V_{net}sin\left(\omega_{net}t + \frac{4}{3}\pi\right). \tag{A.6}$$

The compensation currents are defined through

$$\begin{aligned} i_{comp,a}(t) = \hat{I}_5 sin(5\omega_{net}t + \varphi_5 + \varphi_0) + \\ \hat{I}_7 sin(7\omega_{net}t + \varphi_7 + \varphi_0), \end{aligned} \tag{A.7}$$

$$\begin{aligned} i_{comp,b}(t) = \hat{I}_5 sin\left(5\omega_{net}t + \varphi_5 + \frac{10}{3}\pi + \varphi_0\right) + \\ \hat{I}_7 sin\left(7\omega_{net}t + \varphi_7 + \frac{14}{3}\pi + \varphi_0\right), \end{aligned} \tag{A.8}$$

$$i_{comp,c}(t) = \hat{I}_5 sin\left(5\omega_{net}t + \varphi_5 + \frac{20}{3}\pi + \varphi_0\right) + \hat{I}_7 sin\left(7\omega_{net}t + \varphi_7 + \frac{28}{3}\pi + \varphi_0\right), \tag{A.9}$$

where φ_0 is an additional variable for horizontal phase shift of the compensation currents. The AC power, which must be delivered by the APF DC-link is

$$p_{af}(t) = v_a(t)i_{comp,a}(t) + v_b(t)i_{comp,b}(t) + v_c(t)i_{comp,c}(t). \tag{A.10}$$

Since the used phase voltages are purely sinusoidal and the compensation currents consist of only the 5^{th} and 7^{th} harmonics, the resulting $p_{af}(t)$ is a purely sinusoidal signal with a frequency of $6f_{net}$ and amplitude $\hat{p}_{af}$:

$$p_{af}(t) = \hat{p}_{af} sin(6\omega_{net}t) \tag{A.11}$$

The highest value of $\hat{p}_{af}$ appears for $f_{net} = 360Hz$ and $V_{net} = 236V$. That is why the following calculations are done for this operation point. The complete formula for p_{af} in eq. A.10 is quite long. For $\varphi_0 = 0$, the peak power $\hat{p}_{af}$ is at about 0,1 ms as depicted in fig. A.2. To simplify the calculation of $\hat{p}_{af}$, the horizontal position of $\hat{p}_{af}$ is shifted to t=0 through setting $\varphi_0 = 1{,}38rad$ (fig. A.3) (derived empirically). This significantly

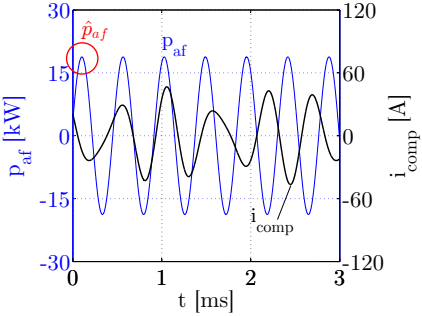


Figure A.2: Compensation current and AC power flow for $\varphi_0 = 0$.

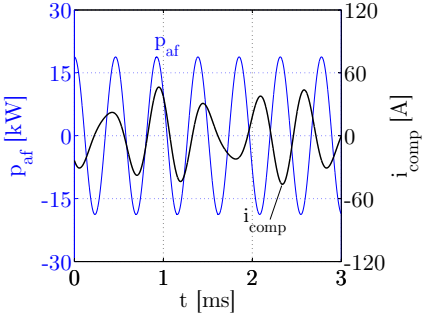


Figure A.3: Compensation current and AC power flow for $\varphi_0 = 1{,}38rad$.

simplifies eq. A.10 to

$$\hat{p}_{af} = \sqrt{\frac{3}{2}}V_{net}\Big[\hat{I}_5 sin(\varphi_5 + \frac{10}{3}\pi) - \hat{I}_5 sin(\varphi_5 + \frac{20}{3}\pi) + \hat{I}_7 sin(\varphi_7 + \frac{14}{3}\pi) + \hat{I}_7 sin(\varphi_7 + \frac{28}{3}\pi)\Big], \tag{A.12}$$

which can be approximated through

$$\hat{p}_{af} \approx V_{net}\left(2.028\hat{I}_5 + 1.086\hat{I}_7\right). \tag{A.13}$$

As already mentioned, the presented formula for $\hat{p}_{af}$ is only valid for $f_{net} = 360Hz$ and $V_{net} = 236V$. $\hat{p}_{af}$ is lower at higher frequency or lower phase voltage.

A.1.3 Derivation of eq. 6.17

The closed loop transfer function for the current control is defined to

$$G_{cc2} = \frac{1}{1 + s\frac{L_{APF}}{K_{cc}} + s^2\frac{L_{APF}T_t}{K_{cc}}} \tag{A.14}$$

(see also eq. 6.16). A second-order transfer function can be described alternatively by

$$G_{cc2} = \frac{1}{1 + s2D_{cc}T_{cc2} + s^2T_{cc2}^2} \tag{A.15}$$

with time constant T_{cc2} and damping D_{cc}. By coefficient comparison

$$\frac{L_{APF}}{K_{cc}} = 2D_{cc}T_{cc2} \tag{A.16}$$

and

$$\frac{L_{APF}T_t}{K_{cc}} = T_{cc2}^2, \tag{A.17}$$

K_{cc} is determined to

$$K_{cc} = \frac{L_{APF}}{4D_{cc}^2T_t} \tag{A.18}$$

and time constant T_{cc2} is determined through

$$T_{cc2} = 2D_{cc}T_t. \tag{A.19}$$

G_{cc2} can be approximated by PT_1 transfer function G_{cc} with

$$G_{cc} = \frac{1}{1 + sT_{cc}}. \tag{A.20}$$

The step response of G_{cc} is

$$h_{cc}(t) = 1 - e^{-\frac{t}{T_{cc}}} \tag{A.21}$$

and the step response of G_{cc2} is

$$h_{cc2}(t) = 1 - \frac{1}{\sqrt{1-D_{cc}^2}} e^{-\frac{D}{T_{cc2}}t} \sin\left[\frac{\sqrt{1-D_{cc}^2}}{T_{cc2}}t + \arcsin\sqrt{1-D_{cc}^2}\right]. \tag{A.22}$$

G_{cc} is an approximation of G_{cc2}. To determine T_{cc}, the area between $h_{cc}(t)$ and $h_{cc2}(t)$ in the range from 0 to ∞ shall be zero (fig. A.4). This is expressed by

$$\int_0^\infty \Big(h_{cc}(t) - h_{cc2}(t)\Big)dt \stackrel{!}{=} 0. \tag{A.23}$$

The resulting T_{cc} is determined numerically to

$$T_{cc} = \sqrt{2}T_{cc2} = 2\sqrt{2}D_{cc}T_t. \tag{A.24}$$

The step responses of G_{cc} and G_{cc2} are depicted in fig. A.4.

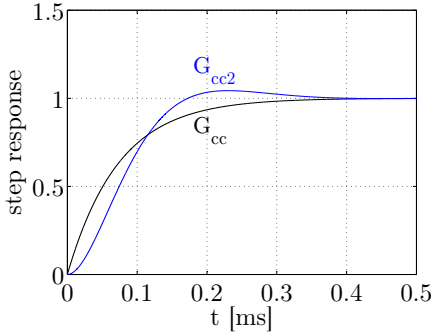


Figure A.4: Comparison of step responses of G_{cc} and G_{cc2}.

A.1.4 Derivation of eq. 6.54

The PLL uses the phase-to-phase voltages for the synchronization. The conversion into the α-β coordination system is done by

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} \tag{A.25}$$

The voltages v_α and v_β in time domain are

$$v_\alpha = \sqrt{\frac{3}{2}}\hat{v}_{ab} sin(\omega_{net} t) = 3V_{net} sin(\omega_{net} t) \tag{A.26}$$

and

$$v_\beta = 3V_{net} cos(\omega_{net} t) \tag{A.27}$$

with RMS phase voltage V_{net}.

The voltage V_q is derived from the Park transformation:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} sin(\omega_{pll} t + \varphi) & cos(\omega_{pll} t + \varphi) \\ -cos(\omega_{pll} t + \varphi) & sin(\omega_{pll} t + \varphi) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{A.28}$$

V_q can be developed to

$$\begin{aligned} V_q &= -v_\alpha cos(\omega_{pll} t + \varphi) + v_\beta sin(\omega_{pll} t + \varphi) \\ &= 3V_{net}\Big[- sin(\omega_{net} t) cos(\omega_{PLL} t + \varphi) + cos(\omega_{net} t) sin(\omega_{pll} t + \varphi)\Big]. \end{aligned} \tag{A.29}$$

The trigonometric rules allow the following relation:

$$\begin{aligned} &sin(\omega_{net} t) cos(\omega_{pll} t + \varphi) \\ &= \frac{1}{2}\Big[sin(\omega_{net} t - \omega_{pll} t - \varphi) + sin(\omega_{net} t + \omega_{pll} t + \varphi)\Big] \end{aligned} \tag{A.30}$$

If the PLL is synchronized with the supply ($\omega_{pll} = \omega_{net}$), this relation can be simplified to

$$sin(\omega_{net} t) cos(\omega_{pll} t + \varphi) = \frac{1}{2}\Big[sin(-\varphi) + sin(2\omega_{net} t + \varphi)\Big]. \tag{A.31}$$

Considering the relation in eq. A.31, eq. A.29 can be further simplified:

$$\begin{aligned} V_q &= \frac{3}{2} V_{net}\Big[- sin(-\varphi) - sin(2\omega_{net} t + \varphi) + sin(\varphi) + sin(2\omega_{net} t + \varphi)\Big] \\ &= \frac{3}{2} V_{net}\Big[- sin(-\varphi) + sin(\varphi)\Big] \end{aligned} \tag{A.32}$$

With trigonometric relation $-sin(-\varphi) = sin(\varphi)$, V_q is

$$V_q = 3V_{net}sin(\varphi). \tag{A.33}$$

A.1.5 Derivation of eq. 6.22

The simplest first order Laplace transfer function is

$$G = \frac{1}{1+sT} \tag{A.34}$$

with corresponding damping function

$$D = \frac{1}{G} = 1 + sT \tag{A.35}$$

and amplitude

$$\big|D\big| = \sqrt{1+\omega^2 T^2}. \tag{A.36}$$

The desired time constant is then

$$T = \sqrt{\frac{D^2-1}{\omega^2}}. \tag{A.37}$$

A.1.6 Derivation of eq. 6.26

During the load dump, the load power characteristic can be simply expressed by

$$p_{load}(t) = \frac{P_{nom}}{2}\big(1 - sgn(t)\big). \tag{A.38}$$

Due to low pass filter T_{2IP}, the calculated instantaneous power $p_{IP}(t)$ in the APF controller has a delay and is described by

$$p_{IP}(t) = P_{nom}e^{-\frac{t}{T_{2IP}}} \tag{A.39}$$

for $t \geq 0\ s$. The difference between real power $p_{load}(t)$ and calculated power $p_{IP}(t)$ is named $p_z(t)$ and defined by

$$p_z(t) = p_{IP}(t) - p_{load}(t) = P_{nom}e^{-\frac{t}{T_{2IP}}} \tag{A.40}$$

for $t \geq 0\ s$. The total energy, which is fed into the DC-link due to $p_z(t)$ is

$$E = \int_0^\infty P_{nom} e^{-\frac{t}{T_{2IP}}} dt = P_{nom} T_{2IP}. \tag{A.41}$$

By the equation for energy content of a charged capacitance

$$E = \frac{1}{2} C_{dc,af} \left(V_{dc,wC}^2 - V_{ref}^2 \right) \tag{A.42}$$

the final voltage $V_{dc,wC}$ (wC = without control) is derived as

$$V_{dc\_wC} = \sqrt{\frac{2 P_{nom} T_{2IP}}{C_{dc,af}} + V_{ref}^2}. \tag{A.43}$$

A.2 Tables and schematics

A.2.1 Material properties

Properties of semiconductor substrate and baseplate materials taken from [26], [128], [35], [129], [130], [131] and [132].

material	thermal conductivity $\left[\frac{W}{mK}\right]$	thermal expansion $\left[\frac{ppm}{K}\right]$	thermal capacity $\left[\frac{J}{m^3K}\right]$	Young's modulus $[GPa]$	dielectric strength $\left[\frac{kV}{mm}\right]$	bending strength $[MPa]$
Chip						
Si	148	2,6	1650	162	30	
SiC 4H	370	4,3		501	300	
Substrate						
Al_2O_3	26	7,1	3020	370	15	350
AlN	180	4,7	2440	308	20	360
Si_3N_4	90	2,5	2100	300	18	650
BeO	250	5,9			10	250
Epoxyd	3,0				60	
Polyimid	0,39				291	
Baseplate						
Al	208	26	2430	70		
Cu	398	17	3450	120		
Mo	138	5,1	2550			
AlSiC	200	7,5	2210			

Table A.1: Properties of materials for power modules.

A.2.2 Characterization results of power semiconductors

Parameter	datasheet	measurement	chosen value for loss calculation
E_{on} [mJ]	12,0	5,18	12,0
E_{off} [mJ]	5,00	4,1	5,00
V_{test} [V]	600	600	600
I_{test} [A]	100	100	100
E_{rr} [mJ]	-	3,04	-
$V_{test,Err}$ [V]	-	600	-
$I_{test,Err}$ [A]	-	100	-
$E_{rr1,end}$ [mJ]	-	3,72	-
i_{rr1} [A]	-	59,0	-
E_{rr2} [A]	-	2,42	2,42
$I_{test,Err2}$ [A]	-	50	50
$V_{test,Err2}$ [V]	-	600	600
V_{ce0} [V]	2,18	1,70	2,18
r_{ce} [mΩ]	17,2	20,9	20,9
V_{f0} [V]	1,3	1,1	1,3
r_f [mΩ]	9,4	11,7	11,7
$R_{thJC,S}$	0,19	-	-
$R_{thJC,D}$	0,9	-	-
$R_{thJCP,S}$	-	0,24	0,24
$R_{thJCP,D}$	-	0,59	0,59

Table A.2: Characterization results of NPT-IGBT module with standard diode.

Parameter	datasheet	measurement	chosen value for loss calculation
E_{on} [mJ]	1,19	0,63	0,63
E_{off} [mJ]	0,63	0,41	0,41
V_{test} [V]	1200	600	600
I_{test} [A]	40	30	30
E_{rr} [mJ]	-	0,28	-
$V_{test,Err}$ [V]	-	600	-
$I_{test,Err}$ [A]	-	100	-
E_{rr2} [A]	-	0,28	0,28
$V_{test,Err2}$ [V]	-	600	600
$I_{test,Err2}$ [A]	-	100	100
R_{ds} [mΩ]	61,0	58,4	61,0
V_{f0} [V]	0,8	0,8	0,8
r_f [mΩ]	75,0	65,0	75,0
$R_{thJC,S}$	0,43	-	-
$R_{thJC,D}$	0,63	-	-
$R_{thJCP,S}$	-	0,52	0,52
$R_{thJCP,D}$	-	0,64	0,64

Table A.3: Characterization results of SiC-MOSFET module with SiC-diodes.

A.2.3 Simulink simulation model

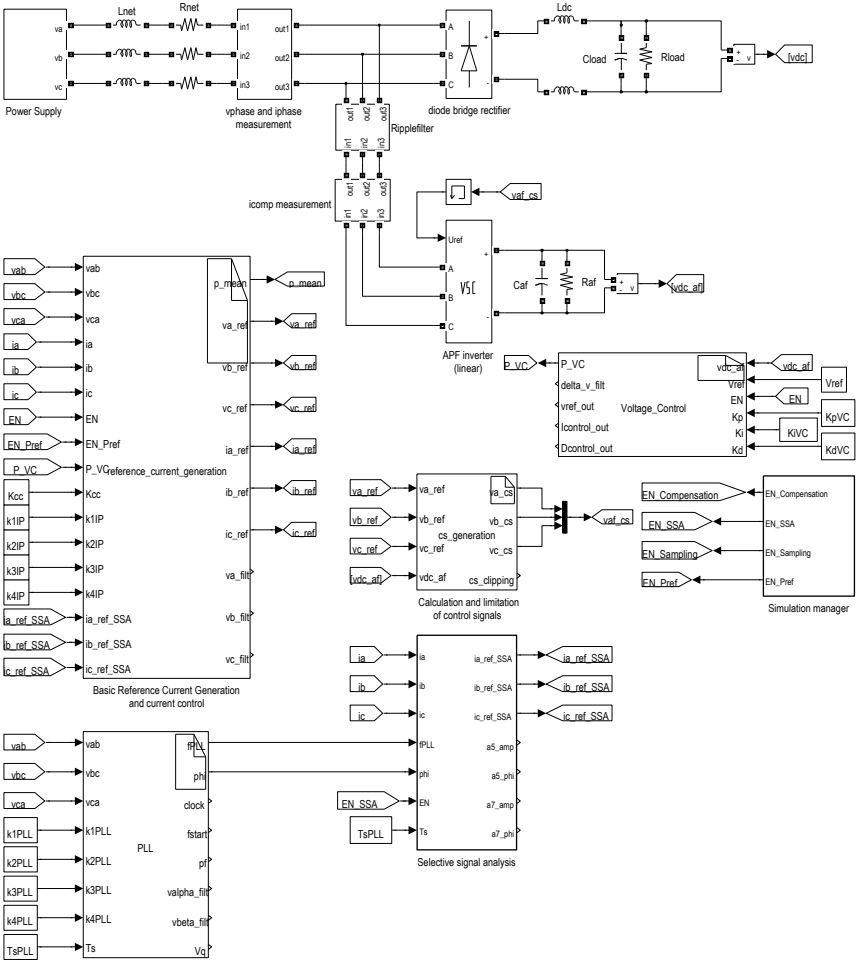


Figure A.5: Simulation model in Matlab / Simulink. All parameters are defined in a m-file.

A.3 Datasheets

A.3.1 Power analyzer LMG500

ZES ZIMMER Electronic Systems

1 bis 8 Kanal Präzisions-Leistungsmessgerät LMG500

- 0,03% Genauigkeit
- 10MHz Bandbreite (DC/0,05Hz bis 10MHz)
- 3 MSamples/s
- Abtastung absolut lückenlos mit Auswertung aller Abtastwerte, dadurch Erfassung aller Einschaltströme und Signaländerungen
- Oberschwingungen und Zwischenharmonische bis 50kHz/1,5MHz
- Flicker, Wechselwirkungen von Netz und Verbraucher

Optimierung Ihrer Motoren, Transformatoren,
Frequenzumrichter, Leistungselektronik,
Stromversorgungen, Leuchtmittel, Fahrzeugtechnik
in Wirkungsgrad, Zuverlässigkeit,
elektromagnetischer Verträglichkeit und Life-Cycle Costs

LMG500-d.12.07

LMG – Ein Synonym für Präzisions-Leistungsmessung

Präzisions-**L**eistungs**M**ess**G**eräte der Serie **LMG** von ZES ZIMMER – LMG90 und LMG95 für 1-phasige, LMG310, LMG450 und **LMG500** für mehrphasige Messung haben sich in mannigfaltigem Einsatz bewährt. Die Zeichenfolge **LMG** ist ein Synonym für die genaue und breitbandige Messung der elektrischen Leistung. Die mit der elektrischen Leistung korrelierten Größen Strom, Spannung, Oberschwingungen, Flicker und Energie müssen genau erfasst werden, um eine Produktoptimierung in Wirkungsgrad, Zuverlässigkeit, Elektromagnetischer Verträglichkeit (EMC), Life-Cycle Costs zu erreichen.

Messungen mit LMGs werden durchgeführt an:

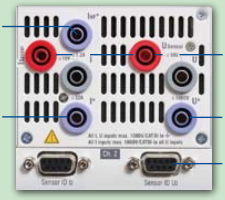
- Bauteilen und Komponenten, z. B. Ferritkernen, Halbleitern, Kondensatoren
- Geräten (Motoren, Invertern, Leuchtmittel)
- Anlagen und Anlagenteilen
- CE zu prüfenden Geräten, versorgt durch Leistungsquelle (ideales Netz), zur Bestimmung der Rückwirkungen durch Stromoberschwingungen und Flicker (Lastschwankungen)
- Netzen und Verbrauchen zur Bestimmung ihrer Wechselwirkungen

Die wichtigsten Leistungseigenschaften des LMG500:

- Laufzeitdifferenz zwischen U- und I-Messeingang standardmäßig <3ns, sehr genaue Messung bei kleinem cosφ und/oder hohen Frequenzen
- Hohe Bereichsdynamik, 3V bis 1000V/3200V_{peak}, 20mA bis 32A/120A_{peak} in direkter Messung jeweils über nur ein Buchsenpaar
- 3MSamples/s, absolut lückenlose Abtastung mit Auswertung aller Abtastwerte
- Erfassung der Transienten und schnellen Signaländerungen mit der im Hintergrund des „Normal-Modus“ laufenden Ereignistriggerung
- Oberschwingungen und Zwischenharmonische bis zu 50kHz im Gerät und bis zu 1,5MHz mit externem PC
- Flickermessung (Wechselwirkungen zwischen Netz und Verbrauchern)
- Modular mit 1 bis 8 Leistungsmesskanälen
- Ergonomische Benutzeroberfläche für leichte, intuitive Gerätebedienung
- Echtzeitvisualisierung der Messungen in Zahlentabellen und Diagrammen
- Schnittstellen mit hohem Datendurchsatz (IEEE488, RS232, USB, Ethernet)

Messeingänge für höchste Anforderungen

- **Gesonderte HF-Stromeingänge I_{HF}*: 150mA bis 1,2A/DC bis 10MHz**
- **Stromeingänge I*, hohe Bereichsdynamik: 20mA bis 32A/120A_{peak} Lästiges Wechseln von externen Shunts entfällt!**



- **Messen über externe Sensoren: Eingänge I_{Sensor} und U_{Sensor} 30mV bis 4V/DC bis 10MHz**
- **Spannungseingänge U*: 3V bis 1000V/3200V_{peak}**
- **Hilfsspannung ±15V und Identifikation externer Sensoren**

- **Erdkapazität der Messeingänge <30pF, dadurch keine Verfälschung der Messsignale**
- **Hohe Bandbreite 10MHz, kürzeste gepulste Signale werden genau gemessen**
- **Alle U-/I-Messeingänge potentialgetrennt gegeneinander und gegen Erde (max. 1000V/CAT III)**
- **Lückenloses Abtasten und Auswerten mit 3MSamples/s bei beliebiger Messdauer, Messzyklus max. 60s**
- **Bis zu 8 Leistungsmesskanäle mit 8 Kanal Kompaktgerät oder durch Zusammenschalten von zwei LMG500, alle Kanäle immer in synchroner Abtastung mit 3MSamples/s**

Spannungsmessbereiche U*												
Nennwert Messbereich /V	3	6	12,5	25	60	130	250	400	600	1000		
Zulässiger Effektivwert /V	3,6	7,2	14,4	30	66	136	270	560	999	1001		
Zul. Spitzenwert für Vollaussteuerung /V	6	12	25	50	100	200	400	800	1600	3200		
Eingangswiderstand	>4,5MΩ || <3pF											
Strommessbereiche I*												
Nennwert Messbereich /A	20m	40m	80m	150m	300m	600m	1,2	2,5	5	10	20	32
Zulässiger Effektivwert /A	37m	75m	150m	300m	600m	1,25	2,5	5	10	20	32	32
Zul. Spitzenwert für Vollaussteuerung /A	56m	112m	224m	469m	938m	1,875	3,75	7,5	15	30	60	120
Shuntwiderstand		560mΩ			68mΩ			7,5mΩ			2mΩ	
Strommessbereiche I_{HF}*												
Nennwert Messbereich /A	150m	300m	600m	1,2								
Zulässiger Effektivwert /A	225m	450m	900m	1,8								
Zul. Spitzenwert für Vollaussteuerung /A	313m	625m	1,25	2,5								
Shuntwiderstand	0,1Ω											
Sensoreingänge U_{Sensor}, I_{Sensor}												
Nennwert Messbereich /V	30m	60m	120m	250m	500m	1	2	4				
Zulässiger Effektivwert /V	37m	75m	150m	300m	600m	1,2	2,5	5				
Zul. Spitzenwert für Vollaussteuerung /V	62m	125m	250m	500m	1	2	4	8				
Eingangswiderstand	100kΩ || 34pF											

Figure A.6: Measurement ranges (extract of LMG500 datasheet).

Messunsicherheit		± (% vom Messwert + % vom Messbereich)										
		DC	0.05Hz..45Hz	**45Hz..65Hz**	65Hz..3kHz	3kHz..15kHz	15kHz..100kHz	100kHz..500kHz	500kHz..1MHz	1MHz .. 3MHz	3MHz .. 10MHz
Spannung	U*	0.02+0.06	0.02+0.03	**0.01+0.02**	0.02+0.03	0.03+0.06	0.1+0.2	0.5+1.0	0.5+1.0	3+3	f/1MHz*1.2 + f/1MHz*1.2
	Usensor	0.02+0.06	0.015+0.03	**0.01+0.02**	0.015+0.03	0.03+0.06	0.2+0.4	0.4+0.8	0.4+0.8	f/1MHz*0.7 + f/1MHz*1.5	f/1MHz*0.7 + f/1MHz*1.5
Strom	I* (20mA .. 5A)	0.02+0.06	0.015+0.03	**0.01+0.02**	0.015+0.03	0.03+0.06	0.2+0.4	0.5+1.0	0.5+1.0	f/1MHz*1 + f/1MHz*2	-
	I* (10A .. 32A)					0.1+0.2	0.3+0.6	f/100kHz*0.8 + f/100kHz*1.2	-	-	-
	I HF					0.03+0.06	0.2+0.4	0.5+1.0	0.5+1.0	f/1MHz*1 + f/1MHz*2	-
	I sensor					0.03+0.06	0.2+0.4	0.4+0.8	0.4+0.8	f/1MHz*0.7 + f/1MHz*1.5	f/1MHz*0.7 + f/1MHz*1.5
Wirkleistung	U* / I* (20mA .. 5A)	0.032+0.06	0.028+0.03	**0.016+0.02**	0.028+0.03	0.048+0.06	0.24+0.3	0.8+1.0	0.8+1.0	f/1MHz*3.2 + f/1MHz*2.5	-
	U* / I* (10A .. 32A)					0.104+0.13	0.32+0.4	f/100kHz*1 + f/100kHz*1.1	-	-	-
	U* / I HF					0.048+0.06	0.24+0.3	0.8+1.0	0.8+1.0	f/1MHz*3.2 + f/1MHz*2.5	-
	U* / I sensor					0.048+0.06	0.24+0.3	0.72+0.9	0.72+0.9	f/1MHz*3 + f/1MHz*2.3	f/1MHz*1.5 + f/1MHz*1.4
	U sensor / I* (20mA .. 5A)		0.024+0.03		0.024+0.03	0.048+0.06	0.32+0.4	0.72+0.9	0.72+0.9	f/1MHz*1.4 + f/1MHz*1.8	-
	U sensor / I* (10A .. 32A)					0.104+0.13	0.4+0.5	f/100kHz*1 + f/100kHz*1	-	-	-
	U sensor / I HF					0.048+0.06	0.32+0.4	0.72+0.9	0.72+0.9	f/1MHz*1.4 + f/1MHz*2	-
	U sensor / Isensor					0.048+0.06	0.32+0.4	0.64+0.8	0.64+0.8	f/1MHz*1.12 + f/1MHz*1.5	f/1MHz*1.12 + f/1MHz*1.5

Figure A.7: Measurement uncertainties (extract of LMG500 datasheet).

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Abbreviated Curriculum Vitae

General

Name	Sebastian Liebig
Nationality	German
Date of birth	10^{th} of March 1982
Place of birth	Munich, Germany

Education

02/2010 - 11/2014	PhD studies at Liebherr Elektronik GmbH and TU Chemnitz
09/2003 - 06/2007	Studies of electrical engineering at University of Applied Sciences Constance
2002 - 2003	Military service
2000 - 2002	Fachoberschule Bad Neustadt a. d. Saale
	Graduation: vocational baccalaureate diploma (Fachabitur)
1992 - 2000	Franz-Miltenberger-Gymnasium Bad Brückenau
	12^{th} grade of school successfully finished

Professional experience

since 07/2007	Power electronics engineer in Advance Development Department of Liebherr Elektronik GmbH

Lindau, May 2015