

# INTERNATIONAL SYMPOSIUM ON DEVELOPMENT METHODOLOGY



## Drive Inverter Testing with Virtual E-Motors Using Power Hardware-in-the-Loop Emulation Concept

Dr.-Ing. Alexander Schmitt, Dipl.-Ing. Horst Hammerer, Dr.-Ing. Patrick Winzer, Dr.-Ing. Mathias Schnarrenberger – AVL SET GmbH



## Abstract

Electrical power trains are part of safety-critical vehicle functionality. The challenge is to increase test quality and test depth without increasing test effort, while the scope of functionality is increasing and development times are becoming shorter. A new method where the real e-motor is replaced by an e-motor-emulator allows load and ambient conditions to be reproduced in the laboratory exactly as they occur in a drive inverter during a real-life driving situation: A Power-HIL System using a virtual e-motor.

E-motor-emulators meet the demands of development-related tasks, verification on hardware, software and system level. At the same time requirements stipulated by ISO 26262 including fault injection or fault stimulation can be fulfilled. Conventional inverter test methods using real e-motors and mechanical testbeds are not designed for fault injection or fault stimulation. An e-motor-emulator (EME) however, provides full reproducibility of fault scenarios without endangering the unit under test (UUT).

The Power-Hardware-in-the-Loop (PHIL) setup makes it possible to visualize high-dynamic processes, independent of mechanical limitations. As the e-motor is not present as a mechanical device/application but exists in form of software models, motor parameter settings are adjustable and can be altered easily – even during testing.

This new test methodology allows an extremely fast inverter test process flow saving more than 90% of the testing time compared to other approaches.

Leading companies of the worldwide automotive industry have already taken advantage of the benefits of testing drive inverters without a real e-motor. The field of application ranges from typical inverter R&D testing up to field return analysis.

For the daily routine of development and testing e-motor-emulation implies that inverters and new electrical drive concepts can be tested under full power, without the necessity of having the future e-motor physically present. This permits the decoupling and parallelization of many tasks in the development process of drive systems, leading to considerable time and cost advantages.

## **1** Introduction

Modern electric cars contain increasingly more number of power electronic components that are all part of safety-critical vehicle functionalities (see <u>Figure 1</u>). Within an electric car, the powertrain inverter seems to be the most complex and delicate device. In analogy to the combustion engine of a conventional powertrain architecture, the inverter in an electric vehicle acts as the "power processor", transforming electrical energy into torque via an electric actuator (e-motor) in a closed loop control scheme. In addition, "standard" torque control, specific functions like electrical braking and ABS (anti-lock braking system) can be part of the inverter software – making this device one of the most complex and safety-critical parts in an electric car.

The classical approach to the development of an electric car and its components (e.g. inverter) follows the well-established V-model shown in <u>Figure 2</u>a. However, the V-model has some drawbacks. The most critical one among the others is, that all testing and integration tasks are not started until all components are developed and the engineering process has been completed. However, this could give the impression, that the development phase ends with a fully



Figure 1: Overview of the power electronic components in an electric car





a) Established V-model

b) New W-model with dedicated test process Figure 2: Development processes for electric cars



Figure 3: Typical failure costs in a development process

operational product. A planned removal phase for defects and regression tests is not considered in the V-model [1].

Furthermore, the main challenge in nowadays development processes is to increase the scope of functionality and complexity while keeping the development time as short as possible. Due to this, agile or test-driven development methods are becoming more and more popular [2]. As a result, even the well-established V-model has meanwhile been optimized and extended to the W-model shown in Figure 2b. Thereby, the W-model addresses the same drawbacks as the agile or test-driven methods and is basically a V-model extended by a parallel process "V" for test strategies and test tools (see Figure. 2b). The goal of this extension is to create a dedicated test strategy for any requirement of every component and system of the car.

The trend towards improved test strategies is supported by the fact, that failure costs increase dramatically as the development process progresses (see <u>Figure 3</u>). Thus, failures must be identified and removed as soon as possible. The ideal test and validation zone is therefore the engineering phase.

To be able to cope with all of these requirements, the test methods and test strategies of modern electrical cars - especially with respect to drive inverters - have to be strongly improved.

A new dedicated test method for drive inverters that fulfills all the aforementioned requirements is introduced in this paper. This new test method not only allows realistic drive-, load- and ambient test conditions, but also allows tests to be carried out in an early engineering phase, exactly as they occur in an inverter's life cycle. The paper starts with a brief overview of conventional inverter testing by means of a rotating motor testbed as well as Signal Level Hardware-inthe-Loop (SHIL) testbeds (chapter 2). The differentiation of the HIL test architectures in SHIL (signal level) and PHIL (power level) has become important with the introduction of power electronic units like drive inverters. Subsequently, the new dedicated inverter test system, as well as its basic functionality are introduced in chapter 3. Different test categories and various test cases where this method can be used are presented in chapter 4. Conclusions and an outlook on the potential of this new inverter testbed are stated in chapter 5.





a) Signal Level Hardware-in-the-Loop testbed

b) Conventional motor testbed

Figure 4: Conventional testbeds for drive inverter testing

## 2 Conventional inverter test method

According to the V-model, inverter testing is already a part of drive train integration. Therefore, the first holistic inverter tests are often executed on a rotating motor testbed (see Figure 4b). During the actual development process, inverters are commonly tested only by means of Signal Level Hardware-in-the-Loop test systems (SHIL) (see Figure 4a). As for inverter tests however, SHIL tests have several disadvantages. Since these systems cannot validate thermal influences, electromagnetic interferences (EMI) or durability of the inverter, they allow only partial inverter tests [3]. Furthermore, a very critical drawback of the SHIL methodology for drive inverters is the dramatic modification of the unit under test (UUT) in order to keep signal level restrictions: All power paths are being disabled, which means that not much hardware is left in the "test loop". This is a fatal situation - in particular, with respect to safety related testing.

Furthermore, even an inverter test on a motor testbed is always a compromise and has several limitations. For instance, all tests can only be conducted when the real motor is already available. This is often not the case, since the motor and the inverter are commonly developed in parallel. Moreover, due to fabrication tolerances of the electric motor, test conditions at these testbeds can vary between technically identical motor load combinations, thus making these tests not 100% reproducible [4]. In addition, exchanging motors is an extensive task and several motor test benches are needed to cope with different power demands. Therefore, the space required for testbeds can be large and additional costs and maintenance efforts are inevitable.

Another limitation of rotating testbeds is, that the stored energy within the rotating mass of the machines cannot be controlled in case of a malfunction of the UUT. Due to this, these testbeds cannot protect the UUT (often even a golden sample) against destruction.

Moreover, standard operation points like "hill-stop" or "hillstart" with very low speed and full torque are critical for the inverter and therefore important test cases, that are always troublesome for conventional motor testbeds. These inverter test scenarios are hard to be accomplished on a conventional motor testbed. Any motor testbed – simply spoken – is a drive train, too. However, due to the intrinsic control characteristics and limited bandwidth they have a tendency to oscillate at low speed and high torque. Finally, conventional motor test benches are limited in their fault emulation capability. Faults like a crack of the shaft, a blocking rotor or winding short circuits are very difficult to test.

## 3 Inverter testing using Power Hardware-in-the-Loop concept

On the contrary, Power Level Hardware-in-the-Loop (PHIL) emulation test benches (see <u>Figure 5</u>) allow holistic inverter tests under all possible operating conditions in a very early development stage. These testbeds can precisely mimic arbitrary electric motors using parameters that can be obtained by motor measurements or calculated by means of finite element analysis (FEA). Thus, changing the motor type or parameter set can be executed by software within seconds.

The PHIL setup makes it possible to visualize high-dynamic processes, independent of mechanical limitations. As the e-motor is not present as a mechanical device/application, but exists in form of software models, motor parameter settings are adjustable and can be altered easily – even during operation.

This allows a parallel component development of motor and inverter with full test capability of the inverter before the motor is physically available. Furthermore, PHIL tests are 100% reproducible, since the tolerances of such a testbed are only determined by the accuracy of the used data acquisition, that is why manufacturing tolerances and thermal drifts are negligible. Therefore, the PHIL testbed dramatically lowers the risk of unexpected failures and allows the developers to



Figure 5: Inverter testbed using Power Hardware-in-the-Loop concept [5]



handover a very mature inverter design for the classical system integration.

#### General working principal

Basically, a PHIL emulator consists of three main components (see <u>Figure 5</u>) [5]. First, a high-performance signal processing unit including a data acquisition system is needed to calculate the physical behavior of the real motor quasi-continuously and in real-time. Since an e-motor can be modeled very precisely with a generic motor model, the implementation of the motor model can be done very thoroughly in an Field Programmable Gate Array (FPGA) to minimize the dead times and to increase computation speed as much as possible [6].

In addition, the real-time simulation system emulates the rotor position (y) and speed (n) signals as well as temperature sensors (T) within the e-motor. Identical to real e-machines, the only connections between PHIL and UUT are the three power terminals as well as the position and temperature signals, which in turn excludes any test-driven modifications at the UUT. This is of high relevance for safety related tests as it must be ensured that the UUT shows precisely the same behavior as the unit inside the car. Any modification of the UUT in hardware or software (to make testing easier) violates this fundamental law.

Secondly, the emulator is equipped with an ohmic inductive coupling network as every e-motor is also an ohmic inductive system. Dependent on the performance of the emulator the inductance of the coupling network can be very low, since a high-performance emulator can mimic even the current ripples that occur within the real e-motor. Indeed, a base inductance is always needed as control path.

The third main component of the PHIL system is the emulation converter itself. It is therefore important to use a high-performance emulation converter with a switching and control frequency of several hundred kHz to mimic the impedance with respect to the current trend of the real e-motor quasi-continuously in real-time. Furthermore, this property is mandatory even with a coupling network that fits the inductance of the e-motor, as effects like saturation or cross-coupling occur in every electric motor and have to be emulated precisely. Also, the emulation converter has to be fed by a galvanically isolated power supply since the real machine coils are galvanically isolated too [7, 8].

#### Versatile inverter testbed based on power electronics

Modern e-motor emulators (EME) like the EME of AVL SET fulfill all the mentioned demands and allow verification on hardware, software and system level of inverters in a very early stage. At the same time, requirements stipulated by ISO 26262, including fault injection or fault stimulation can be qualified as well. Furthermore, these EME testbeds provide full reproducibility of fault scenarios without endangering the UUT.

<u>Figure 6</u> depicts a possible variant of the latest inverter testbed from AVL SET. The testbed is specifically designed for a flexible usage during drive inverter development. The testbed consists of two independent three phase EMEs with scalable current ratings from 400A to 1200A. Each EME allows the operation of a UUT with a DC-link voltage up to



Figure 6: Schematic overview of AVL SET's versatile inverter testbed including EME, EME Power Supply (PSU), Battery Emulator (BEM), Failure Insertion Matrix (FIM), Testbed Configuration Matrix (TCM) and Rotor Emulator for Externally Excited Synchronous Machines (EESM-RE)



1000V. The testbed is also equipped with a failure injection matrix (FIM) to test the influence of short circuits or wire breaks on the UUT. On demand, the testbed can be extended by a rotor emulation cabinet (EESM-RE) to emulate not only permanent magnet synchronous machines (PSM) and induction machines (IM) but also externally excited synchronous machines (EESM). As the power topology allows the use of real batteries, the testbed can also be used for integration tests of inverter and battery. Whenever the use of a real battery is out of scope, the modular architecture can be simplified by closing the power path on the DC level. This is accomplished by a set of DC/DC converter modules which replace the battery emulator and the EME PSU. In that case, the power connection to the mains only compensates the system's losses.

The workload of the testbed is increased by a testbed configuration matrix (TCM). The TCM allows combining both EMEs to work in parallel which doubles the phase current capability and the power ratings. Furthermore, both EMEs can be operated to emulate 6-phase e-motors, the latest trend of e-motor topologies. This flexible testbed architecture has been realized, as many test cases do not require a testbed with peak power or peak current. Thus, most of the test cases can be conducted on two independent inverter testbed channels at the same time. This increases the utilization of a single inverter testbed and accelerates the whole testing process. A testbed with full power or full current is only required for some specific performance and fault tests (e.g. short circuits). Due to the testbed architecture, all test cases where the current or power of the motor exceed their nominal values, can be easily conducted on the combined testbed.

The basic performance data of AVL SET's testbeds is shown in Table. 1.

### 4 Different test categories for drive inverters

The W-model (see <u>Figure 2</u>b) states four major test categories during the development process of an electric car. The inverter testbed can support all categories apart from road tests. In everyday practice, the main application area of an inverter testbed is the component test, as this is the most crucial area regarding the inverters functional range. Looking at the product lifecycle, the component test of inverters can be divided into three different test categories (see <u>Figure 8</u>).

First, there are tests during the actual component development phase. These tests usually have an experimental character and therefore require a very flexible and powerful testbed with a lot of variance.

Examples for **development tests** are:

- Controls testing (stability, limitations, parameter tolerances, derating, etc.)
- HW-component testing (cooling, plugs & sockets, sensor interfaces, etc.)
- Fault testing (short circuits, wire breaks, mechanical faults, etc.)
- Operation points (curbstone test, hill-start, drive cycles, etc.)

Subsequently, every specified requirement of the inverter must be validated systematically to provide a technically mature inverter design before the system integration starts. Es-

Parameter	Single testbed	Dual testbed
Max. DC-link Voltage UUT [V]	1000	1000
EME Current 3ph [Arms]	400 / 800 / 1200	800 / 1600 / 2400
EME Current 6ph [Arms]	-	400 / 800 / 1200
Model calculation freq. [MHz]	3.125	3.125
EME Switching freq. [kHz]	800	800
EME max. fundamental freq. [kHz]	5	5
Possible machine types	3ph PSM, IM, EESM	3 & 6ph PSM, IM, EESM

Table 1: Basic performance data of AVL SET's inverter testbeds

A complete inverter testbed requires several additional components beside the components in the power path. For that reason, an inverter testbed is often equipped with a power analyzer, a coolant conditioning system, a climatic chamber and an automation system. An exemplary testbed setup with all these peripheral components is shown in <u>Figure 7</u>. pecially in case of an outsourced inverter development, this task is of crucial importance and must be conducted with utmost care.

#### Examples for **validation tests** are:

- Hardware validation regarding lifetime and reliability:
  i. Highly accelerated life test (HALT test)
  ii. Highly accelerated stress screening (HASS test)
- Second source component qualification (semiconductors, capacitors, sensors, etc.)





Figure 7: Exemplary inverter testbed of AVL SET including additional peripheral components

- Software validation i. Stipulated requirements (e.g. ISO 26262 / ASIL, etc.) ii. Operational strategies (drive cycles, range optimization, etc.)
- Series maintenance (SW-updates, HW-improvements, redesigns, etc.)
- Building block respectively platform maintenance

Finally, a test strategy for end of line tests is required. These tests are very cost sensitive, since a lot of test channels are needed. However, the functional requirements and the flexibility are very low. Examples for **end of line tests** are:

- Functional check (isolation, mounting, etc.)
- Calibration (measurements, interfaces, etc.)
- Safe launch tests

Since these categories in a given context have completely different requirements regarding the performance (power, current, emulation quality, etc.) as well as the needed peripheral components (climatic chamber, HALT / HASS chamber, automation system, etc.), it is important to consider them in the specification of an inverter testbed.





Fig. 8 Different test categories for drive inverters





Whenever actual requirements are taken into account and properly assessed correctly, this new test methodology allows an extremely fast inverter test process flow, saving more than 90% of the testing time compared to other approaches.

## 5 Summary

Modern drive inverters are becoming more and more complex whereas, at the same time, development time and costs must be reduced. This conflict of objectives can only be solved with new development strategies and processes. All established processes show the same limitations regarding testing. Therefore, a new test methodology for drive inverters is presented, that allows comprehensive tests for drive inverters from the very beginning.

This new method, where the real e-motor is replaced with an e-motor emulator, allows not only load and ambient conditions to be reproduced in the laboratory exactly as they occur in a drive inverter during a real-life driving situation, but also save a lot of time and effort as well as increase safety for the system and its user.

The Power-Hardware-in-the-Loop (PHIL) setup from AVL SET makes it possible to visualize high-dynamic processes, independent of mechanical limitations. As the e-motor is not present as a mechanical device/ application but exists in form of software models, motor parameter settings are adjustable and can be altered easily – even during testing.

This new test methodology allows an extremely fast inverter test process flow, saving more than 90% of the testing time compared to other approaches.

Leading companies of the worldwide automotive industry have already taken advantage of the benefits of testing drive inverters without a real e-motor. The field of application ranges from typical inverter R&D testing up to field return analysis.

For the daily routine of development and testing, e-motor emulation implies that inverters and new electrical drive concepts can be tested under full power, without the necessity of having the future e-motor physically present. This permits the decoupling and parallelization of many tasks in the development process of drive systems, leading to considerable time and cost savings.

## References

- [1] A. Spillner, "The W-MODEL Strengthening the Bond Between Development and Test," 2000.
- [2] A. Komus and M. Kuberg, "Status quo agile," in Studie zu Verbreitung und Nutzen agiler Methoden, 2015.
- [3] A. Schmitt, "Hochdynamische power hardwarein-the-loop emulation hochausgenutzter synchronmaschinen mit einem modularen-multiphasen-multilevel umrichter," Dissertation, Karlsruher Institut für Technologie, KIT Scientific Publishing, 2017. [Online]. Available: https://¬publikationen. bibliothek.kit.edu/-1000066073
- [4] IEC, IEC 60034-1, 12th ed. IEC Central Office, 3 rue de Varembé, 1211 Geneva CH, 2010.
- [5] A. Schmitt, J. Richter, M. Braun, and M. Doppelbauer, "Power hardware-in-the-loop emulation of permanent magnet synchronous machines with nonlinear magnetics – concept & verification," in Proceedings of PCIM Europe, May 2016, pp. 393– 400.
- [6] A. Schmitt, J. Richter, U. Jurkewitz, and M. Braun, "Fpga-based real-time simulation of nonlinear permanent magnet synchronous machines for power hardware-in-the-loop emulation systems," in IECON - 40th Annual Conference of the IEEE Industrial Electronics Society, Oct. 2014, pp. 3763–3769.
- [7] A. Schmitt, M. Gommeringer, J. Kolb, and M. Braun, "A high current, high frequency modular multiphase multilevel converter for power hardware-in-the-loop emulation," in Proceedings of PCIM Europe, May 2014, pp. 1537–1544.
- [8] A. Schmitt, M. Gommeringer, C. Rollbühler, P. Pomnitz, and M. Braun, "A novel modulation scheme for a modular multiphase multilevel converter in a power hardware-in-the-loop emulation system," in IECON - 41st Annual Conference of the IEEE Industrial Electronics Society, Nov. 2015, pp. 1276–1281.