Novel Master/Slave Configurated Closed Loop Regulated Modular 320kW Isolated Symmetric CLLC Resonant DC/DC Converter

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***Abstract*—A phase shift modulation based closed loop voltage regulation and current balance scheme is proposed for a high power, modular, multi-power path symmetric isolated bidirectional capacitor-inductor-inductor-capacitor (CLLC) resonant DC/DC converter. Novel master/slave configuration facilitates connection of multiple symmetrical CLLC DC/DC converters either in parallel and/or in series combination to increase the voltage and current rating of the converter cluster. The unique daisy chain formation using optical fiber communication allows connection of up to 4 DC/DC converters in one converter cluster. The proposed control scheme is simulated in Matlab/Simulink©, the dynamic and endurance tests (750hours) carried out on the built 1200V-320kW hardware validates the proposed scheme. The soft switching at a high frequency makes the converter to operate with higher efficiency (up to 98%) at full load, while assuring smaller hardware footprint.**

***Index Terms*—CLLC resonant converter, DCCC, EME,Master slave configuration, Modular converter cluster, OFC, PHIL, multi power path, smaller hardware footprint**

I. Introduction

The power hardware-in-the-loop (PHIL) based electric motor emulator (EME) set up provides a unique platform to test crucial, complex drive inverters of a modern electric car and reduces development time [1], [2]. The PHIL-EME based test system is shown in Fig. 1. The main components are EME, DC/DC converter to supply the EME with high DC voltage, a battery emulator (BE) viz. DC voltage source for the Inverter/unit under test (UUT). The UUT is connected to EME on AC side and to BE on DC side and the power cycle is closed by connecting the two DC supply sources. Additional AC/DC power supply units (PSU) connected provide the loss power of the system. When the emulator works as a motor, the power flow is from inverter to emulator and the power cycle is closed over DC/DC converter and BE, when the emulator works as a generator the power cycle direction is reversed. Such a setup requires a galvanically isolated bidirectional DC/DC converter connected to EME, which carries a high magnitude of current, maintains a constant output DC voltage and is highly efficient. Symmetric capacitor-inductor-inductor-capacitor (CLLC) resonant converter (also known as CLLLC) with the proposed control scheme fulfills the above mentioned requirements with a minimum hardware footprint.

The conventional LLC converters are unidirectional and their operation modes and soft switching behaviors would change when these LLC converters are used in bidirectional applications [3]. CLLC converter's operation modes, design, switching frequency vs voltage transfer gain analysis, and time domain analyis are presented in [3]–[6]. In [7] it is stated that the CLLC resonant converter inherits its soft switching and gain characteristics from the LLC converter topology. Pulse frequency modulated (PFM) CLLC converter topologies are presented in [3]–[5], [8], [9] can achieve soft switching over the entire load range, however, PFM based control scheme requires variation of the switching frequency over a wide range, hence poses design challenges and also voltage transfer gain of the converter drastically decreases at high loads [4], with PFM, steady state performance becomes asymmetrical when voltage range widens [10] and such an asymmetry requires the closed loop control system to be adaptive. With single phase shift (SPS) modulation applied to this topology, the symmetrical operation can be achieved and also SPS modulation scheme is easy to implement. The power flow direction is easily handled by changing the sign of the phase shift angle [10]. The aim of this contribution is to demonstrate the operation of symmetrical CLLC resonant converter in a unique modular master/slave configuration with the phase shift modulation (PSM) voltage and current regulation scheme. The

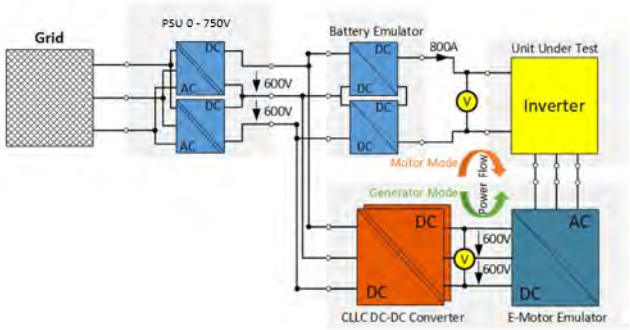


Figure 1. PHIL-EME based inverter test-bed with proposed DC/DC converter cluster.

cluster converter count can be increased up to 8 at present (count can even be upgraded to higher numbers) by which power rating can be increased up to 640kW. In Section 2 the symmetric CLLC resonant converter theory along with the proposed converter cluster is described. In Section 3 master/slave handling mechanism is described, and the proposed control scheme is described in Section 4, in Section 5 and 6 the simulation results and experimental measurement results are presented and finally in Section 7 converter's efficiency and losses are briefly discussed.

II. Resonant Converter based Power Supply System Description

A. Theoretical Background

The symmetric CLLC resonant DC/DC converter simulation model is shown in Fig. 2, converter operates with 50% duty cycle and the switching frequency is maintained at a constant value. The converter consists of resonant inductance $L_r = L_{rp} = L_{rs}$ and capacitance $C_r = C_{rp} = C_{rs}$ along with a 1:1 high frequency transformer with a magnetization inductance of L_m. The power flow is bidirectional and depending upon the direction of the current, one side of the full bridge acts as an inverter and other full bridge acts as a rectifier. The design approaches and analysis of the converter from literature [4], [10], [11] are used in this work for converter modeling and only simplified expressions are presented herewith. First harmonic approximated (FHA) mathematical expressions are as follow: The fundamental square wave input voltage v_{irF} at resonant network is given by

$$v_{irF}(t) = \frac{4}{\pi} V_{in} \sin \omega_s t \tag{1}$$

where V_{in} is the input DC voltage, t is the time and $\omega_s = 2\pi f_s$, and f_s is the switching frequency of the converter. Similarly, the fundamental output square wave voltage v_{orF} of resonant network is given by

$$v_{orF}(t) = \frac{4}{\pi} V_{out} \sin(\omega_s t - \phi) \tag{2}$$

where V_{out} is the output DC voltage and ϕ is the phase shift compared to primary voltage. The fundamental rectifier output current i_{rF} is given by

$$i_{rF}(t) = \sqrt{2} I_{rF} \sin(\omega_s t - \phi) \tag{3}$$

I_{rF} is the rms value of fundamental component of rectifier output current.

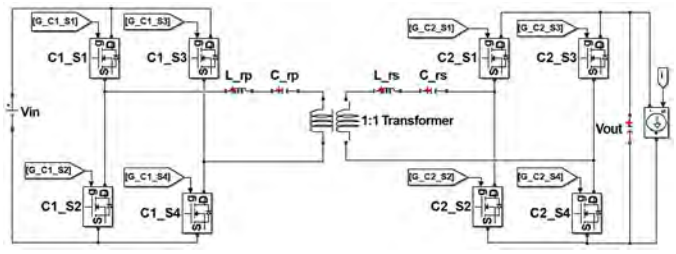


Figure 2. Symmetric CLLC resonant DC/DC converter simulation model.

In order to achieve the soft switching behavior of the CLLC converter in both directions and at a fixed-frequency operation using simple PSM approach resonant components and switching frequency needs to be selected carefully depending upon the voltage transfer gain and load requirements [10]. Compared to conventional resonant tanks this topology offers the following advantages:

- uniform operational characteristics in both forward and reverse power flow direction
- wide input/output voltage ranges possible
- given the symmetrical structure, soft switching is achievable over wide load conditions bidirectionally
- voltage stress on switches are confined to operating voltages without the requirement of additional clamp circuits [4]

The key criterion for soft switching, i.e. zero voltage switching (ZVS) and zero current switching (ZCS) are, ratio of switching frequency (f_s) to series resonance frequency (f_r), voltage transfer ratio (M) and ratio of magnetization inductance to resonance inductance as described in [10].

B. Designed DC/DC Converter Cluster (DCCC)

The DCCC shown in Fig. 3 is designed in such a way that it provides DC link voltage of up to 1200V and is capable of handling total nominal power of 320kW (max. 400kW for 10 minutes). The system comprises of total 4 DC/DC converters, each rated for 800V-100A, 80kW and operate at 70kHz switching frequency. Two individual converters are connected in input parallel output parallel (IPOP) fashion (converter cluster #1) as shown in Fig. 3, operating at 600V to scale the current capacity, and the other identical converter cluster #2 is connected with the converter cluster #1 to form a common mid point to scale the voltage up to 1200V by creating a 3 level voltage bus on both sides. Out of the two parallel connected converters in the cluster, one acts as master and the other as slave.

The master converter control core works as a voltage controller and regulates the output voltage of both the master and the slave to a constant value, using PSM. The current controller implemented on individual converters balance the current flow in the parallel power path (PP). One DCCC can have 4 PPs, the presented system has 2PPs/cluster. The control, modulation, handling and communication actions are implemented on an field programmable gate array (FPGA). Each DC/DC converter module comprises of a control board equipped with an FPGA, a measurement and a communication interface. Fig. 3 shows the broad overview of the control and handling action of the proposed DCCC. The phase shift for the voltage regulation computed by the master controller is communicated to slave controller connected in the daisy chain via optical fiber cable (OFC). The unique handling mechanism facilitates the swapping of master to slave or vice versa.

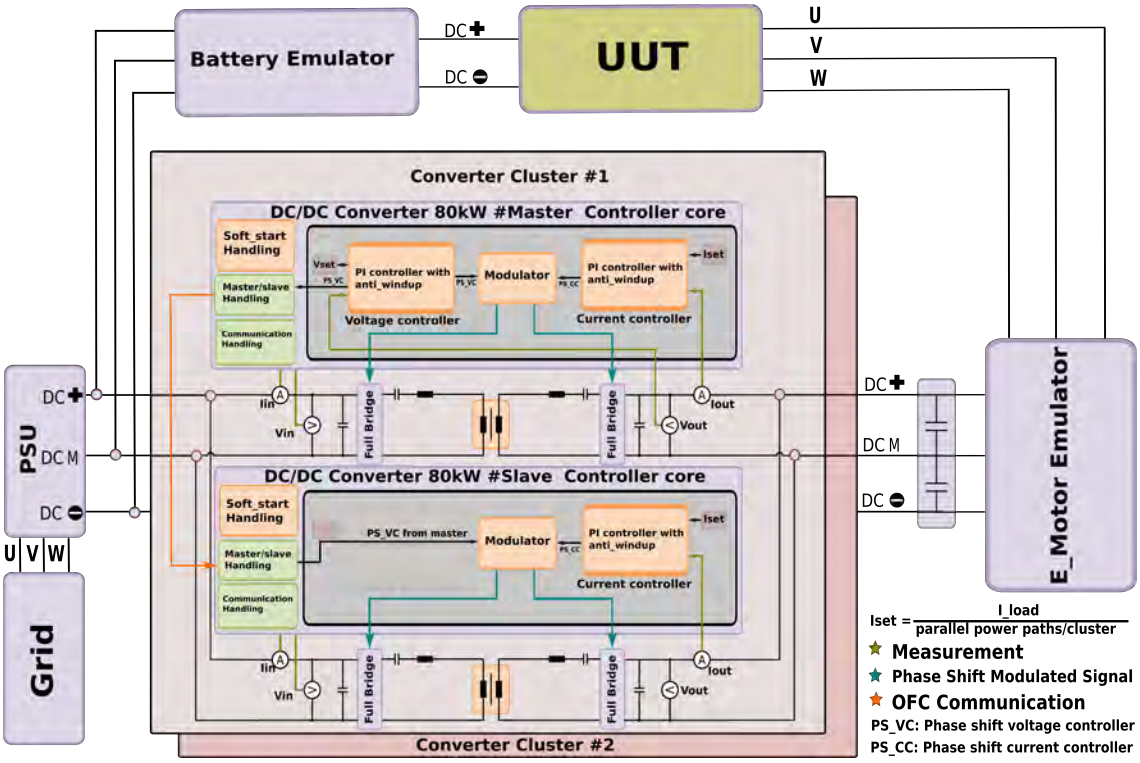


Figure 3. DC/DC converter cluster - Control block diagram.

III. Master/Slave Handling and Communication Mechanism

All OFC communication runs at 3.75Gbit/s. Communication is secured by channel monitoring and checksum handling. Each point-to-point connection causes a latency of about 400ns, but this is acceptable and outweighed by the advantages of the communication method as mentioned here:

- modular and therefore easily scalable system
- high-speed communication
- galvanically isolated interfaces
- low electromagnetic interference (EMI)
- constant latency in the transmission of time-critical messages
- safe and secure transmission channel
- low communication effort for the EME computing platform

Fig. 4 shows the OFC connections between the EME computing platform and one to four DC/DC converters. Each of these converters run with the same firmware on an FPGA. This modular system allows a scalable design with up to four power units without adaptations in software/firmware and all control interface cells are galvanically isolated through OFC communication. Each DC/DC converter is assigned an address when the daisy chain is initialized. The one closest to the platform gets the address zero and is therefore defined as DC/DC master. Those with addresses one to three are the slaves one to three. Calibration with offsets and gains of all measurements, adjustable safety limits for currents and voltages as well as different operating modes are carried out via the computing platform. All set values are stored in an electrically erasable programmable read-only memory (EEPROM) in each DC/DC converter and are reloaded at start-up. The firmware of all FPGAs can also be updated via the platform.

The DC/DC master communicates directly with the EME computing platform. Commands such as the set voltage and power enable are sent from the platform, on the way back the DC/DC master reports the actual states and measured values.

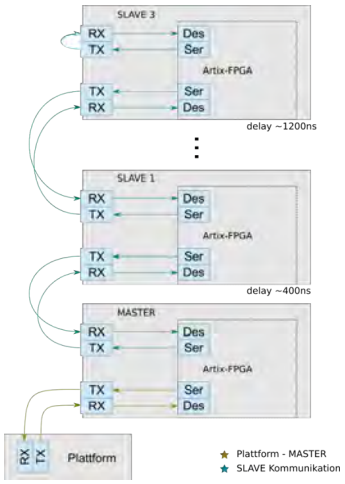


Figure 4. Master/Slave OFC communication scheme.

Based on the addresses used in the daisy chain, the DC/DC master knows how many DC/DC slaves it must control. The master supplies its slaves with the necessary variables and control commands. These in turn send back all measured values and their own status. Slaves connected in the daisy chain do simply pass on information not intended for them. Each FPGA calculates the respective control signals for its PP from the given variables.

IV. The Control and Modulation Scheme

The proposed control scheme utilizes SPS modulation, with a fixed duty cycle of 50%, and the converter is operated at a constant switching frequency. SPS modulation scheme being used to a CLLC resonant converter along with careful selection of resonance components and switching frequency helps in achieving higher efficiency by means of ZVS for primary switches, reducing the turn off current quasi ZCS for secondary side switches. For control action the load side is defined as secondary and the input side as primary. To regulate the output DC voltage of the DCCC, the output DC voltage at the master converter is compared with the set value to compute the required primary to secondary voltage phase shift depending upon the load current direction. This phase shift is directly communicated to slave controller. The master voltage controller output is added with the offset phase shift calculated by the current controller for current balance and the resulting phase shift is fed to the modulator, to generate the required gate pulses.

A. Voltage Control

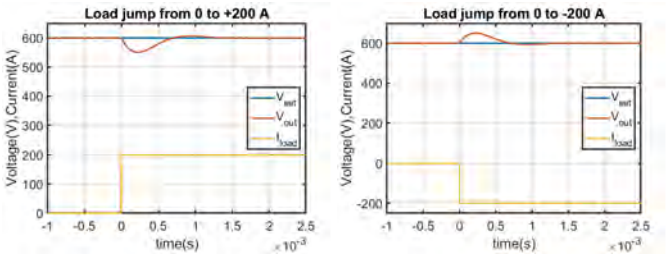
During no load condition primary to secondary voltage phase shift is maintained at near zero value. When a positive load current (primary to secondary) is demanded, the output voltage goes below the set voltage and a proportional integral (PI) based voltage controller introduces a lagging phase shift to regulate the output DC voltage to the set value and the power flow is in positive direction. For a negative load current, the output voltage goes up from the set value, so the controller introduces a leading phase shift to keep the output voltage constant. The update of phase shift is carried out at the rate of switching frequency. A synchronization signal with the same frequency as that of the converter's switching frequency updates the new phase shift angle to the modulator at the beginning of each switching period.

B. Current Balance

In ideal case, where the imbalance factor is zero, the current controller does not produce any offset phase shift, however, the deviation in the inductance or resistance of the PPs introduces an imbalance in the current magnitude that is flowing through each PP. To balance the current, a PI based current controller is employed. Output DC current of each PP is measured and a sum current is calculated, which is then divided by the number of PPs, which is the set current for the controller, based on the magnitude of the DC current flowing through the PP a small amount of offset phase shift is calculated by the current controller, which is added with the phase shift computed by the voltage controller of the master. The current controller only determines the offset phase shift that is required between the master and slave converters.

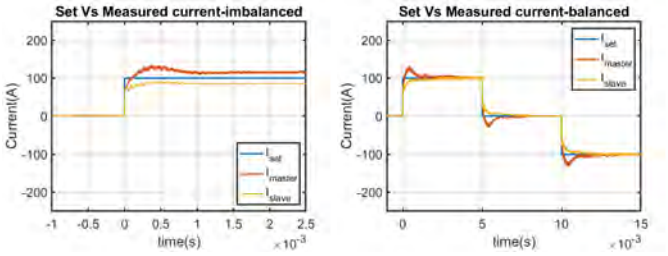
V. Simulation Results

The proposed master/slave configuration of DCCC can provide an output voltage of 1200V and power of 320kW. The simulations are carried out only for the positive leg of the DCCC i.e. two converters connected in parallel providing the DC voltage between DC+ and DC M as shown in Fig. 3, since the converter clusters are connected across common midpoint, the behavior for the DC M to DC- leg remains the same. The dynamic operation points are simulated, and results are presented here. Fig. 5(a) shows the operation of the DCCC at 600V/cluster and a load step change from 0 to 200A (the load is modeled by an ideal current source/sink).



(a) (b)

Figure 5. (a) DCCC voltage regulation at a load jump from no load to 200A (100A/PP) in positive direction, (b) DCCC voltage regulation at a load jump from no load to 200A (100A/PP) in negative direction.

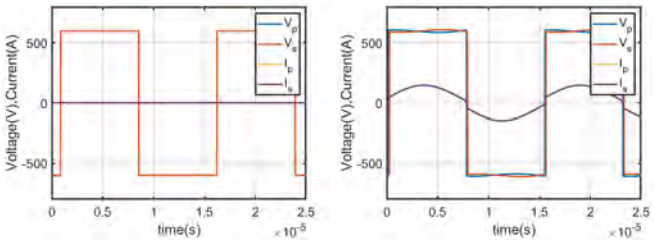


(a) (b)

Figure 6. (a) Imbalanced currents in PPs without current controller, set load current 100A/PP, (b) Balanced currents in PPs with current controller, set load current $\pm$100A/PP.

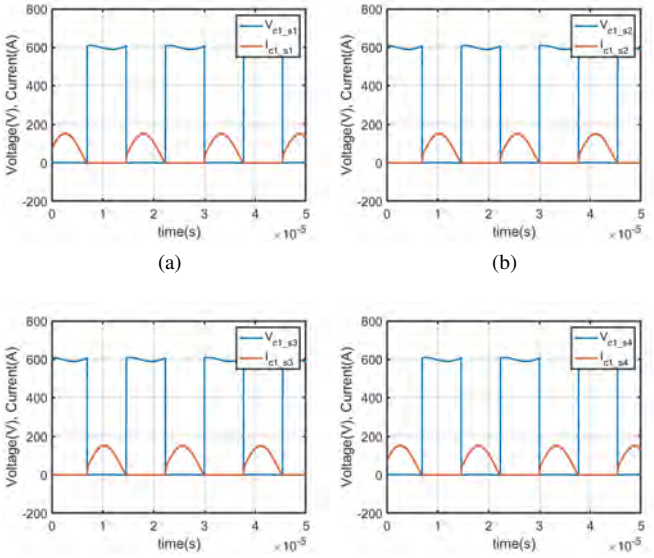
During forward operation the voltage goes below the set point and controller regulates the voltage back to the set value within 1.2 ms and with an 8% undershoot. Similarly, Fig. 5(b) shows the dynamic response of the DCCC while operating at 600V with a load current change from 0 to -200A. Fig. 6(a) shows the DCCC operation without the current controller and an imbalance factor of 20% in L_r, for a demanded 200A load current (100A/PP), it can be seen, that the master converter carries more current as compared to slave because of the reduced reduced impedance in the flow path. Fig. 6(b) shows

the DCCC operating with the same 20% imbalance factor but with the presence of current controller, it can be seen, that current controller balances the current flowing through both the master and the slave. The load current of ±200A (±100A/PP) is carried equally by the master and slave power paths.



(a) (b)

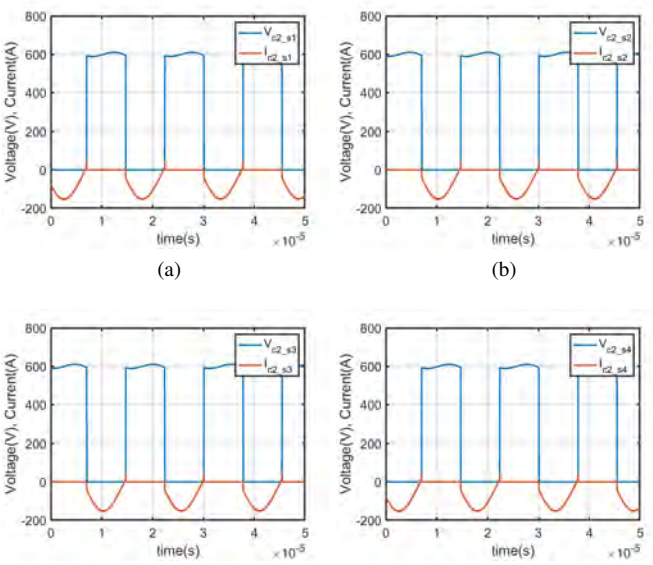
Figure 7. Primary full bridge output voltage, Secondary full bridge input voltage, Current through primary side resonance inductor, Current through secondary side resonance inductor at (a) No load, (b) Load current of +100A/PP



(a) (b) (c) (d)

Figure 8. Converter operating in forward direction at a load of 100A/PP, primary full bridge voltage and current at (a) Switch 1, (b) Switch 2, (c) Switch 3, (d) Switch 4.

Voltage and currents across the converter's primary and secondary side full bridge output and input respectively, are shown in Fig. 7(a) and, Fig. 7(b). When the load current demand is zero, it can be seen from the Fig. 7(a) the primary and secondary side voltages are in phase. In Fig. 7(b) the converter is operating at a load of 100A i.e. 200A/DCCC, during this instance in order to regulate the output voltage a lagging phase shift is introduced between primary and secondary side full bridges and the current lags the primary side voltage hence achieves ZVS for the primary switches. The ZVS behavior of the converter is shown in Fig. 8. Voltage and current at each switches in the primary side full bridge are



(a) (b) (c) (d)

Figure 9. Converter operating in forward direction at a load of 100A/PP, secondary full bridge voltage and current at (a) Switch 1, (b) Switch 2, (c) Switch 3, (d) Switch 4.

shown, when the DCCC is operating at 600V and 100A/PP. Similarly, secondary side full bridge switch voltage and current are shown in Fig. 9. From Fig. 8 it can be seen that each switches on primary side achieve ZVS. The current during turn off is zero as can be seen from Fig. 9, it is evident that secondary side switches achieve quasi ZCS even at high load condition.

VI. Experimanetal Results

In order to validate the proposed configuration and the control scheme, the DCCC is operated at various combinations of input and output voltages and also load conditions. The experimental setup consists of an input DC voltage source (E-storage), DCCC and a controlled current source/sink (I-storage) at the output of the DCCC. The used E-storage has a regulation time of 5ms for a load of 50A. The DCCC output voltage set point is made to follow the output voltage of E-storage in order to maintain the voltage transfer ratio 1.

In Fig. 10 the dynamic response of DCCC operating at 600V is shown, and the current controller is deactivated and a step load change is commanded from -200A to +200A. Even at such high load change, the converter is able to handle the transition smoothly and regulate the output voltage with an undershoot of ∼50V, it is also clear that due to the variation in the power path impedance, the current carried by master and slave vary in magnitude. The primary full bridge voltage (Vp), secondary full bridge voltage (Vs), primary transformer current (Ip) and magnetization current (Im) are shown in Fig. 11, the converter is operating at a switching frequency of 70kHz at 600V and 100A. DCCC dynamic operation points at 400V, 50A/2PP with current controller are shown in Fig. 12. A load jump of -50A to +50A is commanded and the dynamic

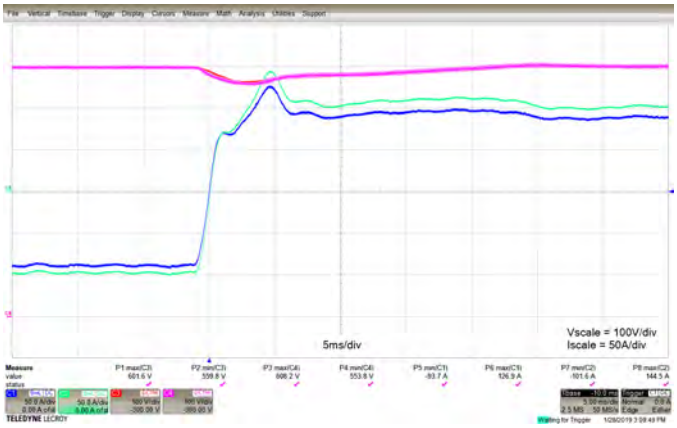


Figure 10. Dynamic Voltage response of DCCC at $V_o = 600V$ Current step -200A to +200A, red-input DC voltage, magenta-output DC voltage, green-master output current, blue-slave output current.

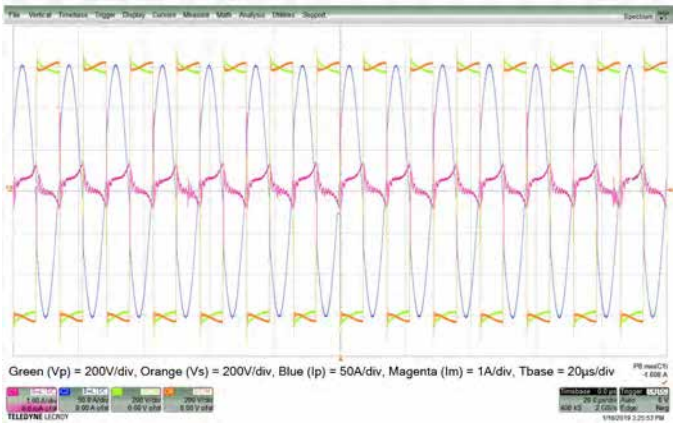
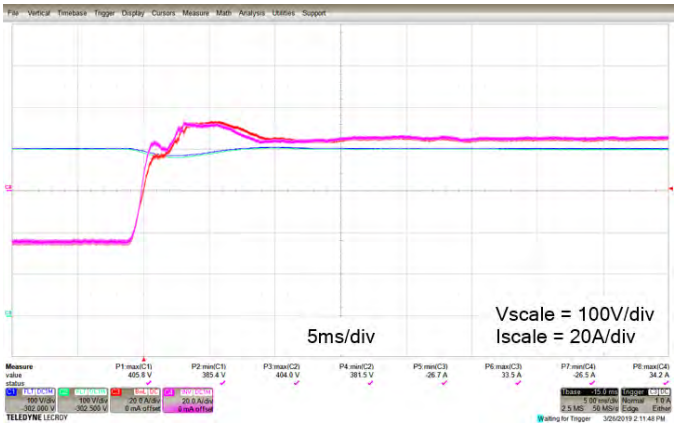


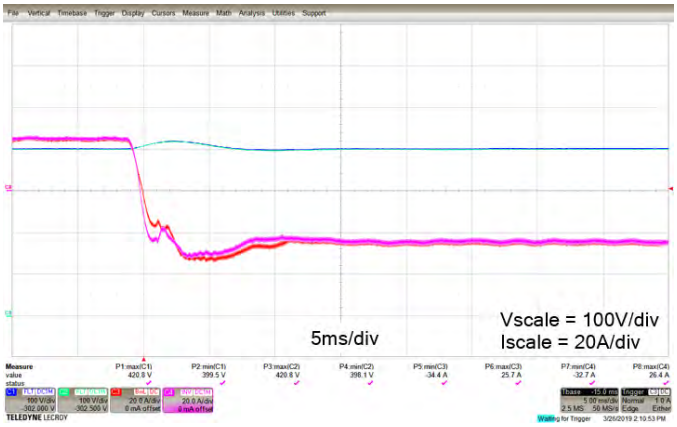
Figure 11. Full bridge voltages, transformer currents at 600V/100A, green-Vp, orange-Vs, blue-Ip, magenta-Im

response is shown in Fig. 12(a), similarly Fig. 12(b) shows the dynamic output regulation when the DCCC operating in forward mode and transits to reverse mode with the commanded current being +50A to -50A, from the dynamic response it is evident that, converter handles the power flow direction change smoothly and regulates output voltage to a constant set point. The overall overshoot/undershoot is confined to $\pm\sim$20V. In order to validate the current controller operation, the DCCC is operated at 500V, without activating the current controller and, an imbalance factor of 5% is introduced by adding additional impedance in one of the power path. The Fig. 13(a) shows that, out of the two parallel connected DC/DC converters there is a mismatch in the current sharing due to variation in the impedance.

In contrast, Fig. 13(b) shows that, the converters operating at the same operation point in the presence of current controller and same imbalance factor, however, the current sharing is equal among the parallel connected converters. In Fig. 13 the current measurement direction is inverted.



(a)



(b)

Figure 12. Dynamic Voltage response of DCCC at $V_o = 400V$ (a) Current step -50A to +50A, (b) Current step +50A to -50A, blue-input DC voltage, green-output DC voltage, red-master output current, magenta-slave output current.

VII. Power Losses and Efficiency

The efficiency of the converter over wide operating voltages and load currents are shown in Fig. 14. At light load conditions switching losses are dominant and as the load increases the efficiency also increases, at high loads the conduction losses are dominant.

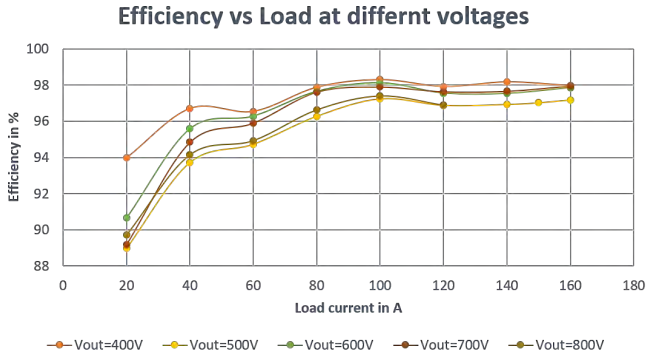
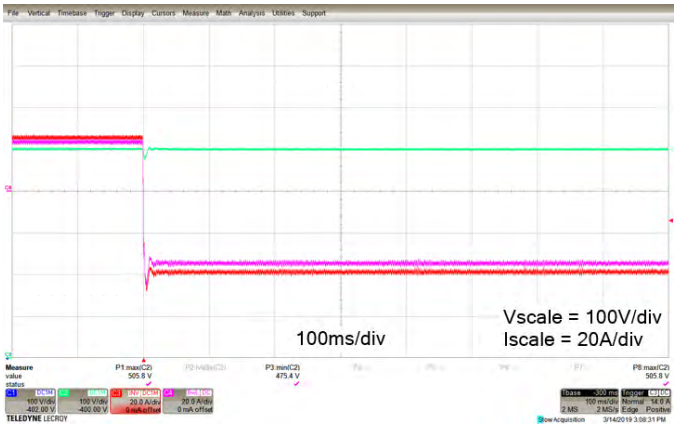
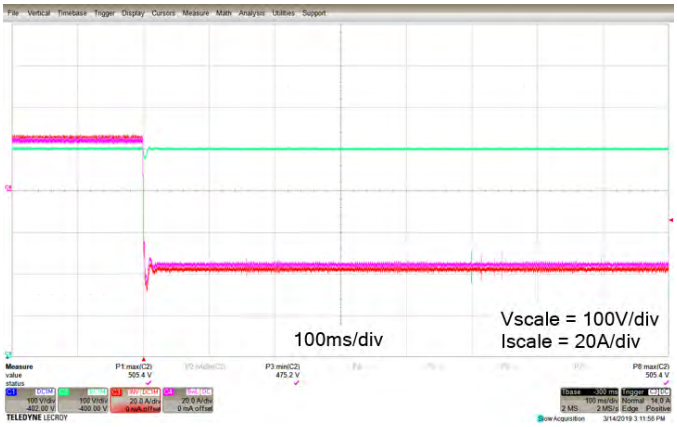


Figure 14. Converter efficiency at different voltages.



(a)

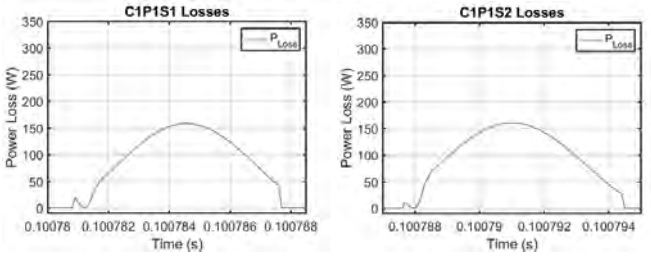


(b)

Figure 13. (a) Imbalanced currents in PP without current controller, set load current 75A/2PP, (b) Balanced currents in PP with current controller, set load current 75A/2PP, green-output DC voltage, red-master output current, magenta-slave output current.

With the given topology ZCS and ZVS are achieved over a wide voltage and load ranges, however, with the increase in the load current, the required phase shift between primary and secondary side to regulate the voltage at the output increases.

With the increase in the phase shift the secondary side switches transition to quasi ZCS region from ZCS region during forward operation, and during reverse operation mode the primary side switches transit to quasi soft switching state. Optimal current waveform, basic ZVS and ZCS topology current waveform given in [12] are used as basis for obtaining overall instantaneous loss curve for each switches. With the decrease in switching frequency further reduction in switching losses is observed, however, the conduction losses tend to increase contributing to the reduction of efficiency at higher loads. Fig. 15(a) and Fig. 15(b) show the instantaneous power losses curves obtained from simulation for the switches S1 and S2 (refer Fig. 2) of the primary side full bridge, when the converter is operating at 70kHz and in forward mode feeding a load of 170A at 600V (overload condition).



(a) (b)

Figure 15. Instantaneous power losses at (a) Switch S1, (b) Switch S2.

VIII. Conclusion

A single phase shift modulated, closed loop voltage and current regulated, symmetrical CLLC resonant converter based DC/DC converter cluster is proposed for high power, bidirectional applications. The simulation results and experimental measurement results from the built hardware are in match and prove the validity of the proposed scheme and novel OFC based master/slave configuration operation, and voltage/power scalability up to 1200V and 640kW. The instantaneous loss curves from simulation and experimental test results at various voltage and load conditions shows the efficient converter operation at wide load ranges. The symmetric resonant topology, high switching frequency operation and soft switching approach helps improve the overall efficiency and to reduce the hardware footprint of the DCCC.

References

[1] A. Schmitt, J. Richter, M. Gommeringer, T. Wersal, and M. Braun, "A novel 100 kw power hardware-in-the-loop emulation test bench for permanent magnet synchronous machines with nonlinear magnetics," in *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, 2016, pp. 1–6.

[2] A. Schmitt, H. Hammerer, P. Winzer, and M. Schnarrenberger, "Drive inverter testing with virtual e-motors using power hardware-in-the-loop emulator concept,," in *AVL 8th International Symposium on Development Methodology*, Nov 2016.

[3] W. Chen, P. Rong, and Z. Lu, "Snubberless bidirectional dc–dc converter with new cllc resonant tank featuring minimized switching loss," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 9, pp. 3075–3086, 2010.

[4] J. Jung, H. Kim, M. Ryu, and J. Baek, "Design methodology of bidirectional cllc resonant converter for high-frequency isolation of dc distribution systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1741–1755, 2013.

[5] J. Lai, L. Zhang, Z. Zahid, N. Tseng, C. Lee, and C. Lin, "A high-efficiency 3.3-kw bidirectional on-board charger," in *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, 2015, pp. 1–5.

[6] S. Ditze, "Steady-state analysis of the bidirectional clllc resonant converter in time domain," in *2014 IEEE 36th International Telecommunications Energy Conference (INTELEC)*, 2014, pp. 1–9.

[7] T. Yu, G. Sicheng, and X. Shaojun, "Research on open-loop soft-start strategy of clllc bi-directional resonant converter," in *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, 2018, pp. 1–6.

[8] W. Chen, S. Wang, X. Hong, Z. Lu, and S. Ye, "Fully soft-switched bidirectional resonant dc-dc converter with a new cllc tank," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 1238–1242.

[9] Z. M. Dalala, Z. U. Zahid, O. S. Saadeh, and J. Lai, "Modeling and controller design of a bidirectional resonant converter battery charger," *IEEE Access*, vol. 6, pp. 23 338–23 350, 2018.

[10] W. Han, R. Mal, and L. Corradini, "Analysis and design methodology for zvs phase shift modulated bidirectional clllc resonant dc-dc converters," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019, pp. P.1–P.10.

[11] M. Jiang and W. Li, "A soft-switching control method of isolated lc series resonant transformer full bridge dc–dc converter," in *Proceedings of the 2013 International Conference on Electrical and Information Technologies for Rail Transportation (EITRT2013)-Volume II*, L. Jia, Z. Liu, Y. Qin, M. Zhao, and L. Diao, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2014, pp. 11–20.

[12] M. Pavlovsky, S. W. H. de Haan, and J. A. Ferreira, "Evaluation of igbt modules and their suitability for zvs, quasi-zcs converter topologies," in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, 2006, pp. 5 pp.–.